



RADC
PRODUCT EVALUATION REPORT
OF THE
AMD Am2903

ICE
INTEGRATED CIRCUIT ENGINEERING CORPORATION
ELECTRONIC KNOWLEDGE FOR INDUSTRY

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PRODUCT EVALUATION REPORT
OF THE
AMD Am2903

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SUMMARY

The purpose of these analyses is to gain first hand knowledge on physical and electrical structuring of these circuits. This permits identifying the strong and weak features of these devices and isolating areas requiring in-depth analysis. In this way a basis will be provided for predicting of circuit reliability and a background will be established for future failure analysis.

The Am2903 4-bit expandable microprocessor slice is made with Schottky bipolar technology with a process that uses washed-emitters, ion-implanted resistors and double-level metallization. The Am2903 contains sixteen internal working registers that may be addressed from two different address buses. The register file may be expanded externally to any number of registers. The Am2903 has a complete arithmetic and logic instruction set. In addition the Am2903 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization and other previously time-consuming operations.

The Am2903 is similar to the Am2901 except the Am2901 cannot expand the internal sixteen-word register file without sacrificing the two-address architecture and shifting capability. Also the Am2901 requires either additional external hardware or additional microinstructions or both to do the single cycle functions built into the Am2903.

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INTRODUCTION

A total of three parts, all purchased from a local distributor and received within six weeks, were used for this analysis. The first two parts marked Am2903DC are commercial temperature range parts and are identified as samples 1E and 2E. The third part, marked Am2903DM, is a military temperature range part and is identified by the sample number 3E.

Interpretation of the device part number is as follows; "Am" indicates Advanced Micro Devices, "2903" is the device type which is a 4-bit expandable microprocessor slice, "D" indicates a hermetic dual-in-line package (DIP), "C" indicates a maximum temperature range of 0°C to +70°C, and "M" indicates the military temperature range of -55°C to +125°C. The packages of the commercial temperature range parts (1E and 2E) were constructed with metal lids and the package of the military temperature range part (3E) was constructed with a ceramic lid.

Samples 1E and 2E both had a date code of 7850 which indicates that assembly was done during the 50th week of 1978. Sample 3E had a date code of 7847 which indicates that assembly was done during the 47th week of 1978. All three samples were marked on the package with a 1978 AMD copyright. All samples received were packed in conductive-plastic packages for static protection.

SECTION I - EXTERNAL PACKAGE ANALYSIS

1.1 - Visual

The Am2903D samples evaluated were packaged in a 48-pin dual-in-line packages. Package photographs of the Am2903DM circuit are shown in Figure 1-1. Examination of Sample 1E, one of the commercial parts, revealed that one of the side-brazed pins was missing. A photograph is shown in Figure 1-2. Examination of sample 2E, revealed that the same pin (pin 11) had a very poor side braze. An equipment malfunction during package construction is suspected. Further examinations showed that the rest of the package was normal, exhibiting no chips in the ceramic or bent leads.

The following statement was received from AMD after AMD reviewed a rough draft copy of this report:

"AMD purchases its side-braze packages from selected suppliers. Our receiving inspection includes a sample verification of pin attachment strength by a 2 Kg stress. As the ICE report suggests the possibility of a recurrent pattern, we have changed our receiving inspection instructions to (1) assure all pin locations are tested in the sample and (2) check for patterns in case of any failures."

Table 1-1 gives a comprehensive listing of the physical measurements.

1.2 - X-Ray

Sample 3E (device Am2903DM) was X-rayed with the results shown in Figure 1-3. This device has a ceramic lid sealed with a glass frit. The X-ray shows that the glass frit is virtually free of voids. The die attach, however, has voids well over 50% of the total die attach area with a major void traversing the width of the chip.

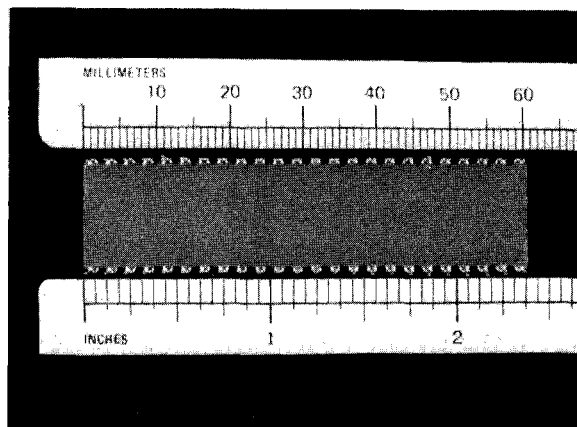
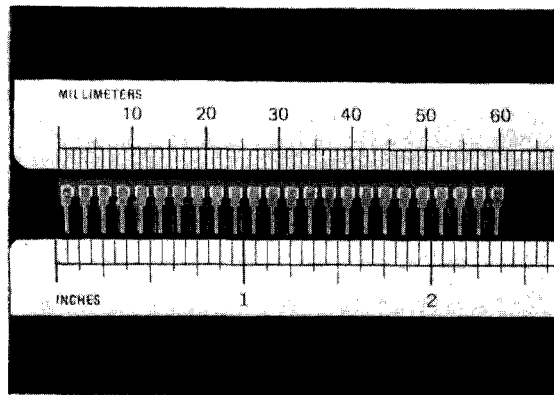
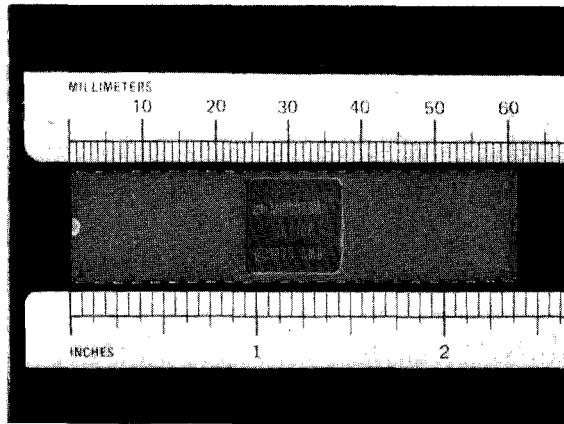


FIGURE 1-1. AMD Am2903 PACKAGE PHOTOGRAPHS.

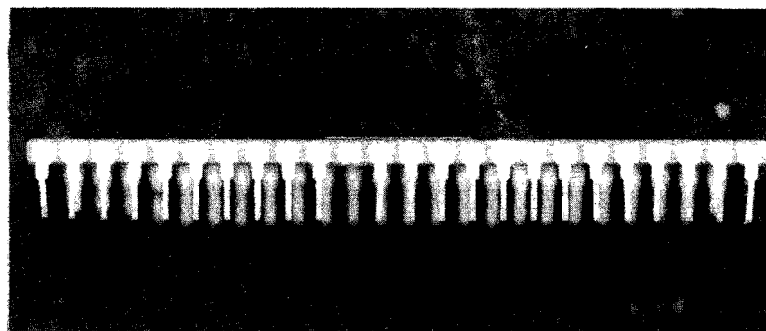


FIGURE 1-2. AMD Am2903 MISSING PIN.

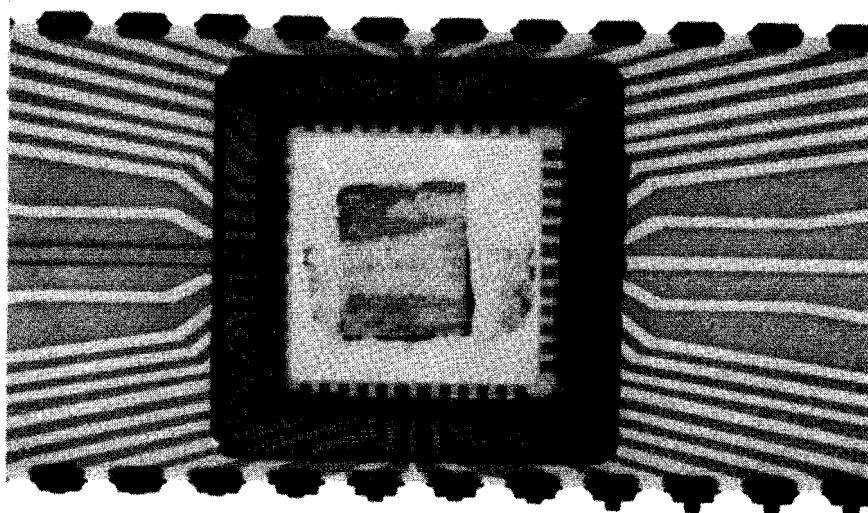
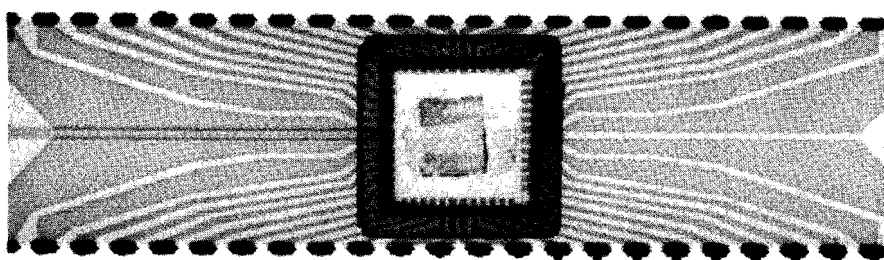


FIGURE 1-3. AMD Am2903 X-RAY PHOTOGRAPHS.

TABLE 1-1

Am2903DM PACKAGE MEASUREMENTS

Package Dimensions:	L 2.4" W .585" T .085"
Package Material:	Dark Ceramic
Number of Pins:	48
Lid Dimensions:	.5" x .5"
Lid Material:	Ceramic
Sealing Method:	Glass Frit Hermetic
Minimum Seal Ring Width:	35 Mils
Cavity Size:	.312" x .312"
Lead Spacings:	.1" x .585"
Lead Material:	Gold-plated Kovar or Alloy 42
Lead Dimensions:	L .13" W .018" T .01"
Lead Attachment Method:	Side-Brazed
Lead Frame Material in Bonding Area:	Gold-Plated.

The large voids in the die attach area should be a reliability concern because of the resulting uneven heat dissipation. The poor thermal conductivity between the chip and the package may cause excessive chip temperatures. The die attach should be monitored as a potential reliability hazard.

1.3 - Leak test and gas analysis

Leak tests were performed on sample 3E (device Am2903DM) per MIL-STD-883B Method 1014.2 Condition B and C. Sample 3E passed both fine and gross leak tests exhibiting a leak rate of less than 1×10^{-8} atm cc/sec.

Gas analysis was done on sample 3E per MIL-STD-883 Method 1018.1 Procedure 1. The results of the gas analysis are shown in Table 1-2. The moisture content was .39%, which is judged to be a safe level. The water vapor content should be no greater than .5% and ideally less than .1%. The amount of CO₂ may be caused by burn-off of an organic binder in the glass frit. The gas analysis would imply that these circuits were sealed in dry ambient air.

TABLE 1-2

GAS ANALYSIS OF THE
Am2903DM (Sample 3E)

CONSTITUENT	CONCENTRATION (% Vol/Vol)
Argon (Ar)	1.07
Carbon Dioxide (CO ₂)	3.34
Oxygen (O ₂)	19.7
Nitrogen (N ₂)	75.4
Water Vapor (H ₂ O)	.39

SECTION II - INTERNAL PACKAGE ANALYSIS

The lid of the Am2903DM was mechanically removed and the die cavity was inspected, according to the procedures described in MIL-STD-883B Method 2010.3 Test Condition B. A comparison to the MIL-STD criteria was not made since this device was not a MIL-inspected circuit, but MIL-STD-883B procedures were used as a guide. Table 2-1 is a comprehensive listing of the internal measurements.

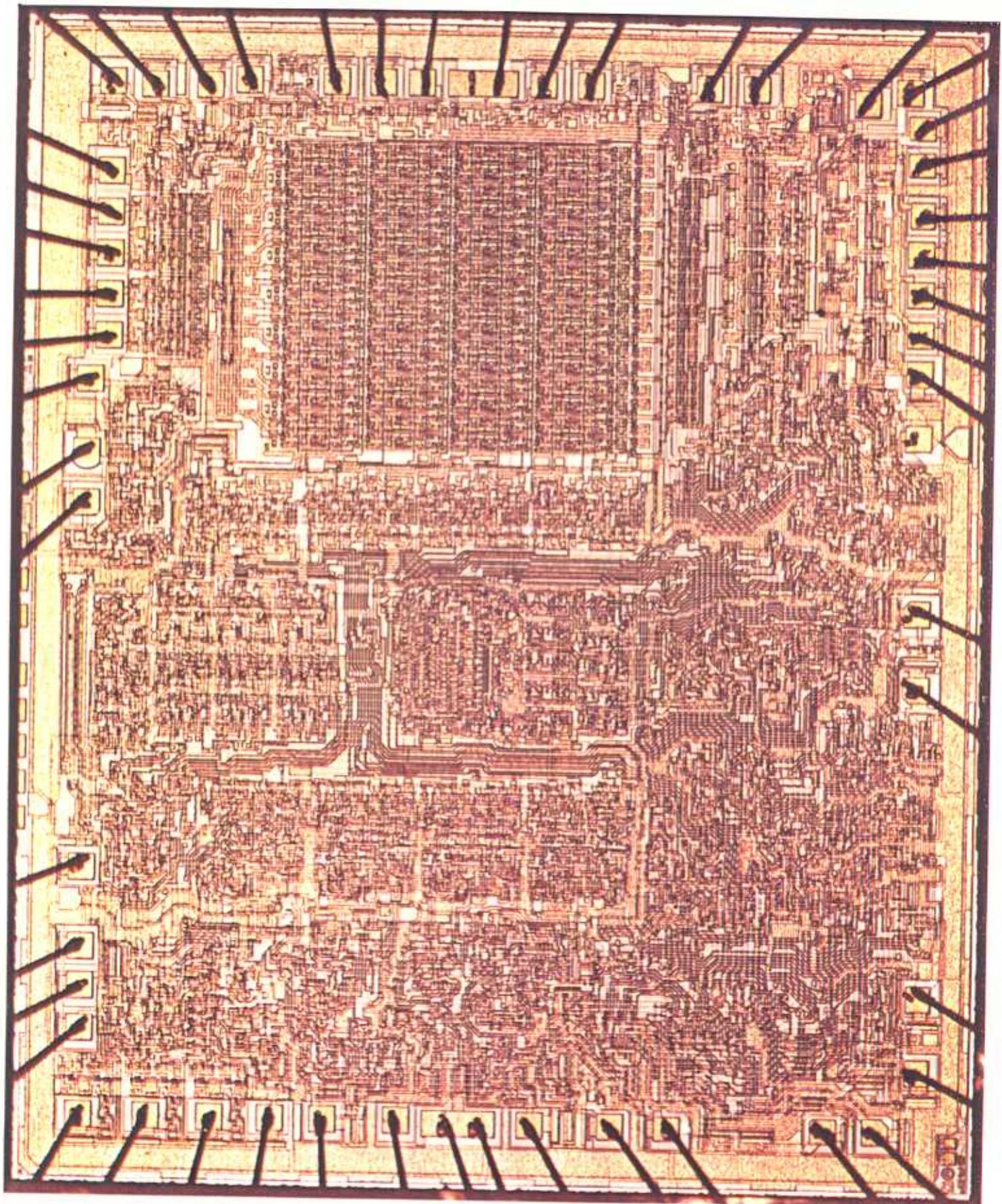
Figure 2-1 is a whole die photograph of the Am2903. A view of the assembled die in the cavity is seen in the SEM photograph of the cavity area in Figure 2-2. There is approximately 50 mils between the cavity wall and the circuit die which provides adequate clearance but still makes it possible to use short bonding wires. The longest span measured was 100 mils.

2.1 - Die Separation and Mounting

The Am2903 die was separated by the saw and break technique as shown in Figure 2-3. Inspection in the SEM disclosed no chips or cracks on the edge of the die extending inwards toward any active circuit element.

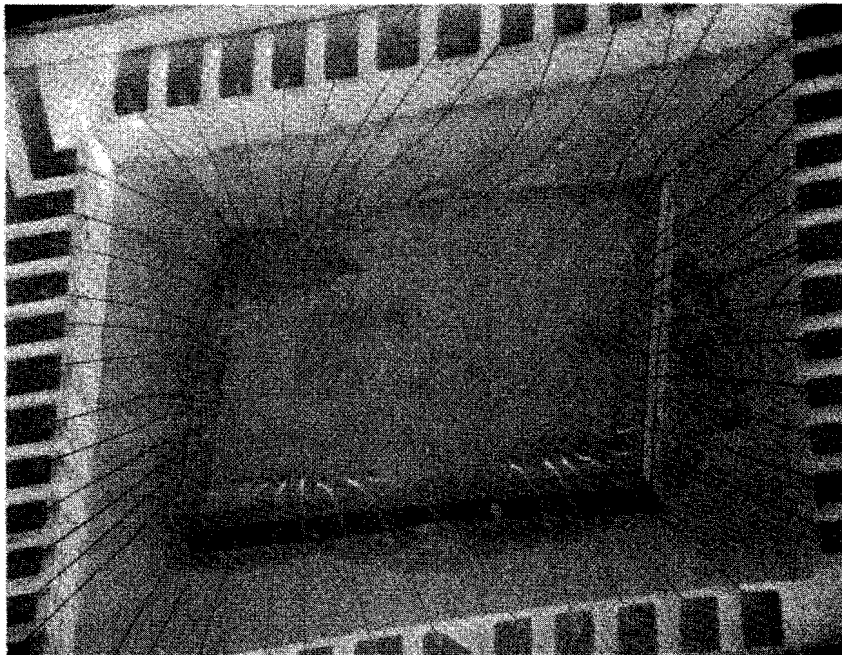
TABLE 2-1
Am2903DM
DIE SPECIFICATIONS

Die Size:	163 mils x 197 mils
Area:	31,752 sq mils
Thickness:	20 mils
Die Separation Technique:	Saw and Break
Die Attach Method:	AuSi Eutectic
Interconnecting Method:	Ultrasonic Wire Bonding
Wire Bonding Material:	Aluminum Size: 1 mil dia.
Longest Span:	100 mils
Minimum Bonding Pad Size:	4.5 mils x 4.5 mils
Minimum Bonding Pad Window:	4.0 mils x 4.0 mils
Minimum Bonding Pad Spacing:	2 mils
Minimum Spacing Pad to Edge of Die:	4.0 mils
Minimum Spacing Pad to Nearest Metal Line:	.8 mils
Minimum Contact Size:	.3 mils x .2 mils
Minimum Diffusion Width:	.3 mils
Minimum Metal Line Width:	.2 mils
Minimum Metal Line Spacing:	.4 mils
Minimum Isolation Width:	.3 mils
Minimum Base to Isolation Spacing:	.3 mils
Minimum Emitter Size:	.3 mils x .2 mils
Bond Strength Test: 48 wires	Sample No.: 2E
Average: 3.39 grams High: 4.5 grams Low: 2.5 grams STD. DEV.: .57 grams	
Die Shear Test: Did not shear at 2500 grams	



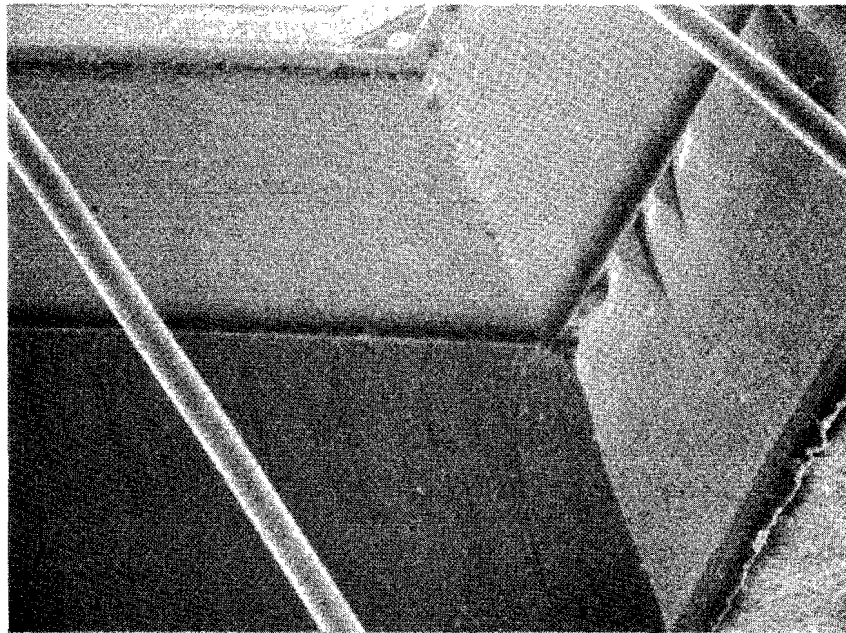
45X

FIGURE 2-1. AMD Am2903 WHOLE DIE PHOTOGRAPH.



15X 45°

FIGURE 2-2. AMD Am2903 DIE CAVITY AREA.



220X 55°

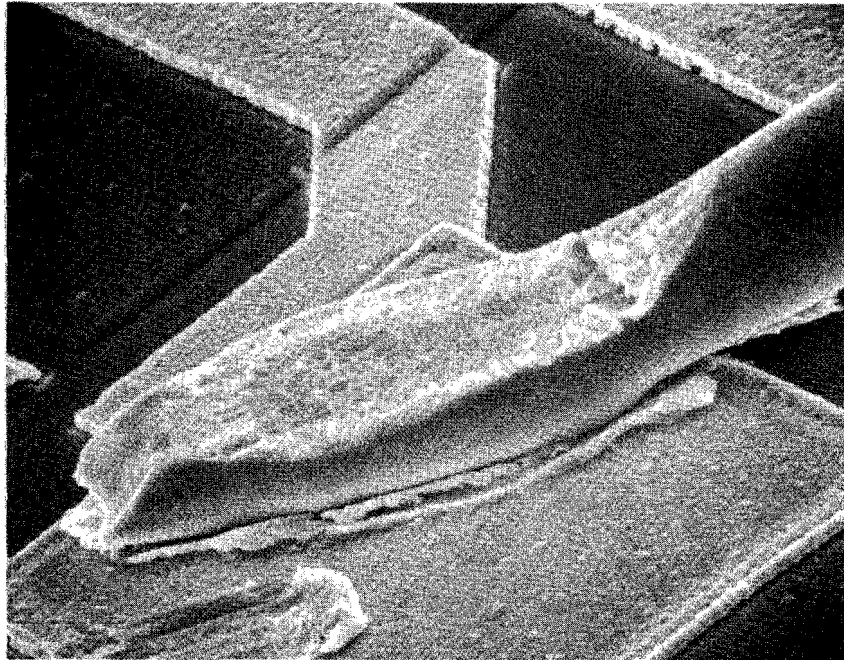
FIGURE 2-3. AMD Am2903 SCRIBE AND BREAK DIE SEPARATION.

Inspection around the perimeter of the chip disclosed no more voids and also found no flaking or balling of the die attach. Sample 3E was subjected to die shear testing. The die did not shear at 2500 grams.

2.2 - Interconnection

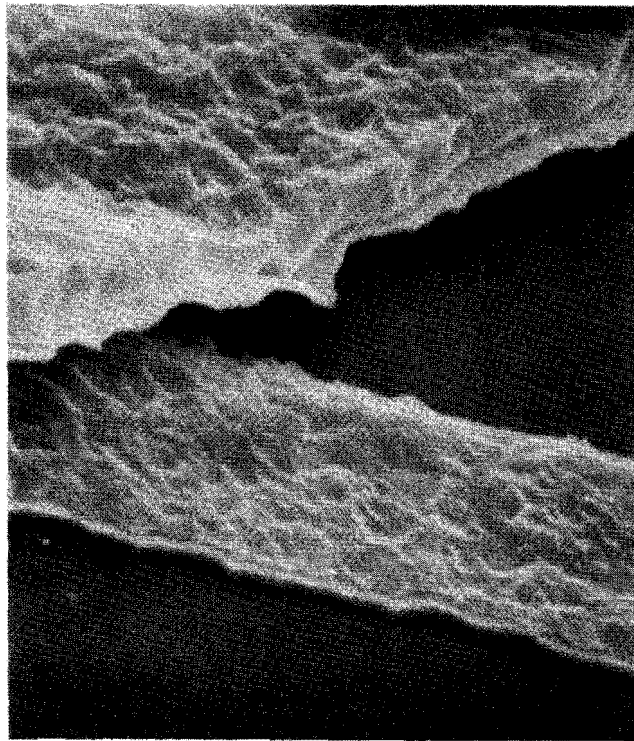
The interconnection method on the Am2903 was ultrasonic wedge bonding. A typical wedge bond is seen in Figure 2-4. The wire used was a 1 mil diameter aluminum wire. The ultrasonic power and the pressure applied was good. A slight squeezing out of the metal was visible underneath the bond but did not look severe enough to cause any reliability problems. Forward bonding was used on this device, which proves to be a good practice in the bonding operation.

Bond strength tests were done on the Am2903. The majority of the wire breaks occurred at the neck down point and in the wire itself. The average bond strength was 3.34 grams and the minimum was 2.5 grams. The minimum post seal strength specified in MIL-STD-883B for this wire is 1.5 grams.



1100X 55°

FIGURE 2-4. AMD Am2903 WIRE BOND.



6000X 55°

FIGURE 2-5. AMD Am2903 METAL STEP COVERAGE.

2.3 - Examination of the Die Surface

Examination of the die surface was done in three steps. First with the glassivation intact, second with the glassivation removed (SEM inspection done at this step), and third with second-level metallization removed. At all three steps no anomalies were found. All spacings and line widths appear adequate for high yields and reliability. The metallization on the Am2903 is both double-level and double-layer. An SEM photograph of the metallization step coverage is shown in Figure 2-5. The step coverage looks normal and no problems were found in this area. X-ray dispersive analysis was used to analyze the composition of the metallization. This analysis indicated that both levels are constructed with aluminum over a tungsten-titanium alloy.

SECTION III - PROCESSING AND ELECTRICAL CHARACTERISTICS

The Am2903 circuit is made with a Schottky-barrier-diode bipolar process incorporating two levels of metal interconnects. Processing techniques used include: Ion-implanted resistors, washed-emitters, possibly composite masking, and multi-layer metallization (two metals in same layer) in addition to the multi-level metallization. A hypothetical process sequence which would produce the visual results observed on the die is as follows:

Table 3-1. Am2903 Postulated Process Sequence.

<u>PROCESS STEP</u>	<u>DESCRIPTION</u>	<u>MASK NUMBER</u>
1.	Buried Layer Masking, Oxide Etch & Diffusion	1
2.	Epitaxial Layer Deposition	
3.	Oxidation	
4.	Composite Mask, Isolation, Bases and Resistors (Body and Ends)	2
5.	Reoxidation	
6.	Isolation Masking (Gross Mask) and Oxide Etch	3
7.	Isolation Diffusion	
8.	Base & Resistor Ends Mask and Oxide Etch	4
9.	P+ Diffusion	
10.	Resistor Mask	5
11.	Resistor Ion-Implant	
12.	Oxidation	
13.	Nitride Deposition	

<u>PROCESS STEP</u>	<u>DESCRIPTION</u>	<u>MASK NUMBER</u>
14.	All Contacts Masking & Nitride Etch	6
15.	N+ Contact Mask (Oversize)	7
16.	N+ Diffusion	
17.	P+ & Schottky Contact Masks (Oversize)	8
18.	Deposit Platinum, Etch Off Excess to form Platinum Silicide in Contact Areas	
19.	Deposit Titanium-Tungsten	
20.	Evaporate Aluminum	
21.	Bottom-Level Intraconnect Pattern Mask & Etch	9
22.	Deposit Oxide	
23.	Mask & Etch VIA Openings	10
24.	Deposit Titanium-Tungsten	
25.	Evaporate Aluminum	
26.	Second-Level Metal Intraconnect Pattern Mask & Etch	11
27.	Deposit Glassivation	
28.	Glassivation Mask & Etch	12

The use of the first composite mask is deduced from the perfect alignment of the body of the resistor to the resistor ends and the lack of any oxide steps outside of the resistor area. The nitride layer is required to continue the composite masking technique to the N+ diffused areas and the contacts.

ICE verified the composition of the metallization by an X-ray dispersive analysis. A barrier metal of titanium-tungsten was used between the platinum silicide and aluminum on both levels of intraconnect. The titanium-tungsten layer was also used in the upper-level of intraconnect.

The washed-emitter process which diffuses the N⁺ dopant for the emitter and collector contacts through the contact openings was definitely used since there was only one cut in the oxide in these contact areas.

SECTION IV - CIRCUIT AND LOGIC ANALYSIS

4.1 - Functional Description

The data sheet provides an excellent description of the architecture of the Am2903. This description includes five tables which show the operation of the instructions that may be generated by instruction inputs I_{0-8} . Some of the features of this architecture will be summarized below.

A functional block diagram of the Am2903 is shown in Figure 4-1. This diagram is the same as that found in the data sheet and was found to be an accurate representation of the circuit. The circuitry that was traced from the chip will be described for each of the blocks in this functional diagram later in this section.

The RAM consists of sixteen registers, each four bits long, which may be addressed from either the A or B address ports.

The Latch at the RAM output port is transparent when the clock input CP is "high" but holds the RAM output data when CP is "low". The RAM output data from the B port may be read at the DB_{0-3} I/O port when the output enable $\overline{OE_B}$ is "low".

The MUX controls the source of the input data to the ALU. The ALU requires data from the R port and the S port. Data into the R port may



come either from RAM output A or DA₀₋₃ input data terminals. Data into the S port may be obtained from any one of three sources: the RAM output B, the Q register or the DB₀₋₃ input data terminals. The ALU may therefore operate on data from two external sources, two internal sources or from an internal and external source.

The Am2903 uses a total of nine instruction inputs. I₀, in conjunction with $\overline{OE_B}$, is used to select one of the three inputs (listed above) to input to the S port. The remaining eight instruction inputs are divided into two groups, one group being I₁₋₄, the other I₅₋₈. The instruction inputs control the ALU functions as well as the ALU Shifter, Q Register and Shifter and the output destination of these logic blocks.

Pin Assignments

The pin assignment of this 48-pin package include the nine instruction inputs, I₀₋₈, two sets of four RAM address inputs, A₀₋₃ and B₀₋₃ which may be used to simultaneously address any two of the sixteen registers. Four data input pins, DA₀₋₃ can be selected by the MUX to input data to the R input of the ALU. The four DB₀₋₃ terminals are I/O pins which may be used to either input data through the MUX to the S port of the ALU or output data from the RAM register addressed by the D₀₋₃ address inputs. The remaining set of four I/O terminals are the Y₀₋₃ pins which are used to input data into the RAM register or output data from the ALU Shifter. Four other I/O terminals include SI₀, SI₃, QI₀, and QI₃. The SI₀ and SI₃ terminals

are bidirectional serial-shift inputs/outputs for the ALU shifter and the QIO₀ and QIO₃ terminals are bidirectional serial-shift inputs/outputs for the Q shifter.

Several ALU functions are determined by four other pins. The C_N terminal is the carry-in input to the ALU. The C_{N+4} terminal is an output which generally indicates the carry-out of the ALU. The $\overline{G}/N$ terminal indicates the carry generate $\overline{G}$ function for the least-significant and intermediate slices. The N function indicates the most-significant-bit of the ALU result of the most-significant-slice. The $\overline{P}/OVR$ terminal is also a dual-function pin which indicates the carry propagate $\overline{P}$ function for the least significant and intermediate slices and indicates the conventional two's-complement overflow OVR signal for the most-significant-slice.

The Z output is an open collector I/O pin which generally indicates the Y₀₋₃ outputs are all "low".

Seven of the remaining pins serve as control functions. Another pin is used for the Clock input and the two remaining pins for the power connections.

Die Partitioning

A die photograph showing the die partitioning is seen in Figure 4-2.

The DB₀₋₃ Output Buffers are located on the upper edge toward the left-hand side of the die directly below the DB₀₋₃ pads. Input address buffers A₀₋₃ and the 1 of 16 decoder connected to the address buffers are located immediately below the output buffers and above the RAM. The output enable buffer ($\overline{OEB}$) for the DB₀₋₃ output stages is located in the upper left-hand corner.

The left-hand side of the die contain the buffer amplifiers for six of the nine Instruction inputs as well as the buffer for the Write Enable input ($\overline{WE}$), the Instruction Enable input ($\overline{IEN}$), the $\overline{LSS}$ input and the $\overline{Write/MSS}$ input/output. The random logic combining the $\overline{LSS}$ and the $\overline{Write/MSS}$ input/output is found above and to the right of these two pads. The input address buffers B₀₋₃ and its associated 1 of 16 decoder is located immediately below the RAM. This circuitry occupies all the space between the RAM and the B₀₋₃ address buffers contain the buffers for the $\overline{CP}$, QI₀, QI₃, and $\overline{EA}$ input and I/O terminals.

The four-bit by sixteen-word RAM is the largest cellular structure on the chip. The Latch and the Write Enable Circuitry is located immediately to the right of the RAM.

Two fairly large circuit functions are located near the Latch. The Q Shifter and Register is located to the right of the lower part of the Latch and the PLA and control circuitry is located to the right of the upper part of the Latch. The MUX and the ALU are located to the right of the Q Register and the PLA.

Other areas containing logic that will be discussed in this report include the upper right-hand corner and the area to the left and above the MUX and ALU. The area in the right-hand corner contains the ALU Shifter and Y Output Buffers. The circuitry identified as the $SI0_0$ and $SI0_3$ functions which contain the parity checker and the $SI0_3$ multiplexer is located to the left of the ALU Shifter and Y Outputs and above the MUX and ALU. This circuitry associated with the Z I/O pin is to the left of the $SI0_0$ and $SI0_3$ circuitry. The remaining circuitry on the chip consists of two areas which contain random control logic circuitry. The area in the upper portion of the die is used primarily to combine instruction inputs I_{5-8} . The area located on the lower right-hand portion of the die contains mostly circuitry that combine instruction inputs I_{0-4} .

Metal Routing

The power leads are routed around the perimeter of the die outside of the bonding pads. Both V_{CC} and ground are in the double-level of metallization in this area. On some parts of the die the top metal is V_{CC} and in other areas, the top metal is ground. Figure 4-3 shows an example of the double-level of metallization and how V_{CC} and ground are interchanged on the two levels of metal. The etch that was used on the metal before this photograph was taken attacked the aluminum layer that is on both the top and bottom levels of metal. When aluminum is etched away, only a very thin layer of titanium-tungsten remains. This layer may be identified in the photograph as the white areas. These areas identify a single-level of metal that may be either the top level or the bottom level. The dark areas show where both levels of metal exist.

Figure 4-3 shows that both levels of metal are at ground potential at the outer edge of this strip. It is believed that this technique was used to provide greater current carrying capacity for the ground bus as compared to V_{CC} bus, rather than for any shielding purposes.

4.2 - Input Address Buffers

The photograph and schematic diagram for Input Address Buffer A_3 is shown in Figure 4-4. Similar input address buffers are used for the A_{0-3} inputs and the B_{0-3} inputs. These buffers provide both the inverting and the non-inverting outputs. These input buffers are also similar

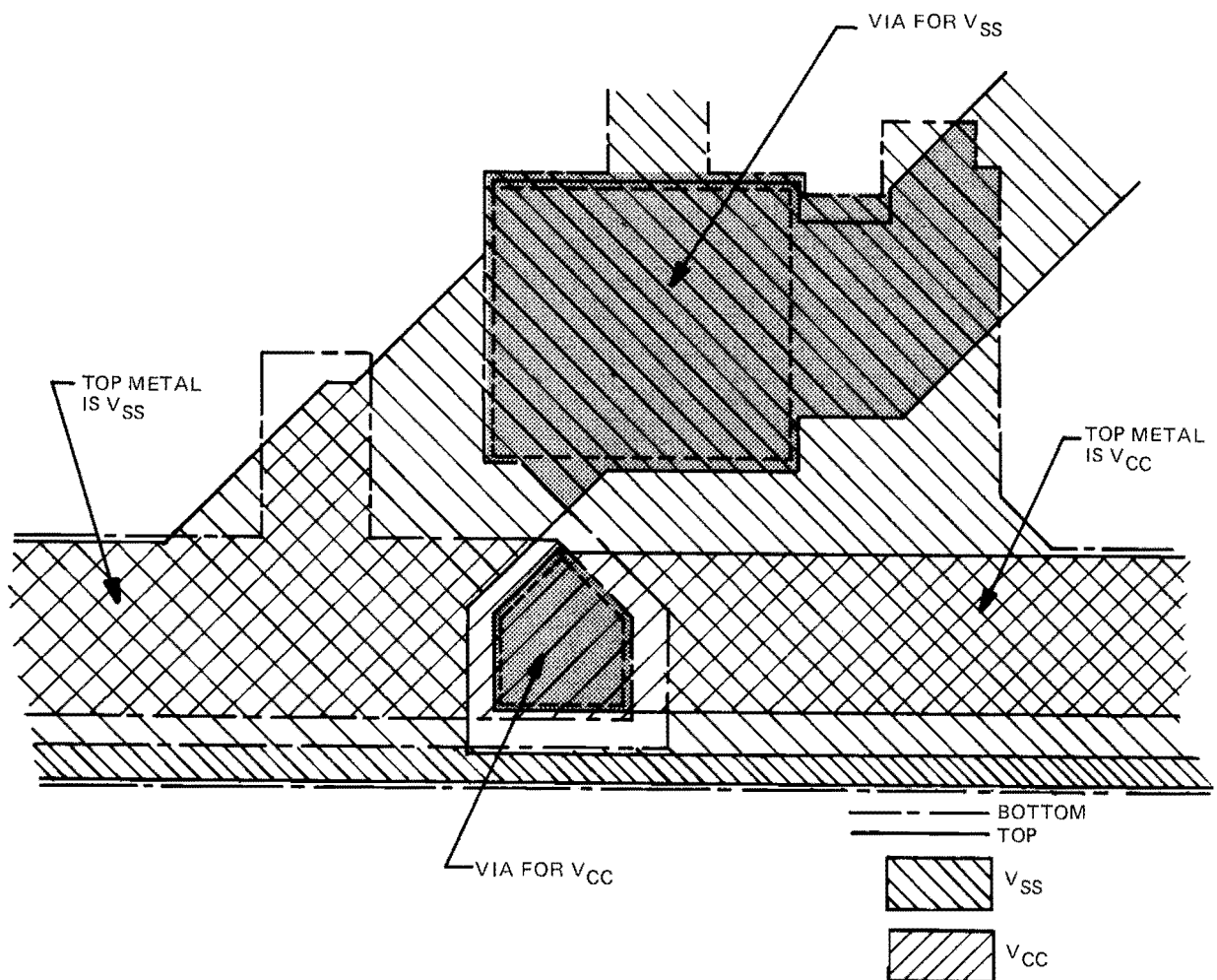
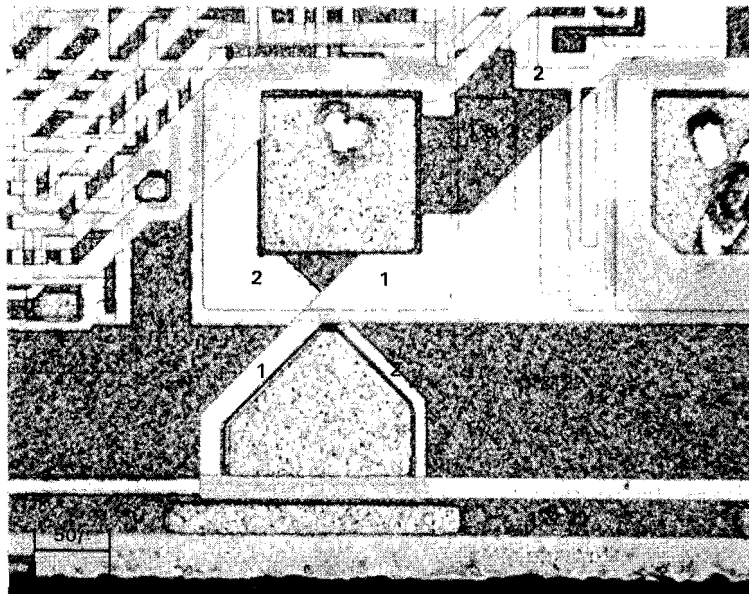


FIGURE 4-3. AMD Am2903 ROUTING OF DOUBLE-LEVEL METAL.

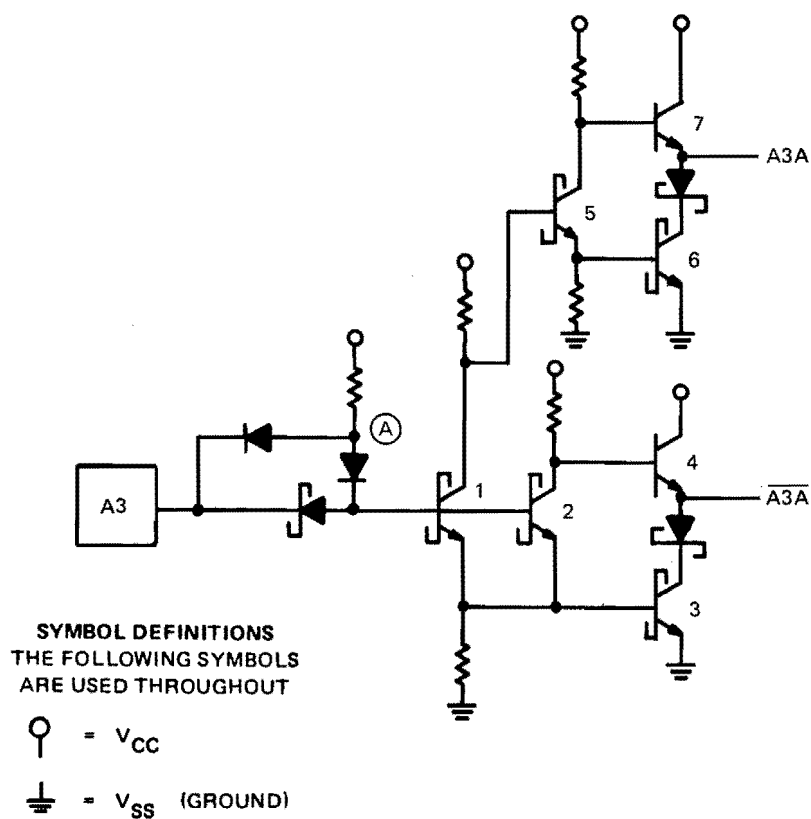
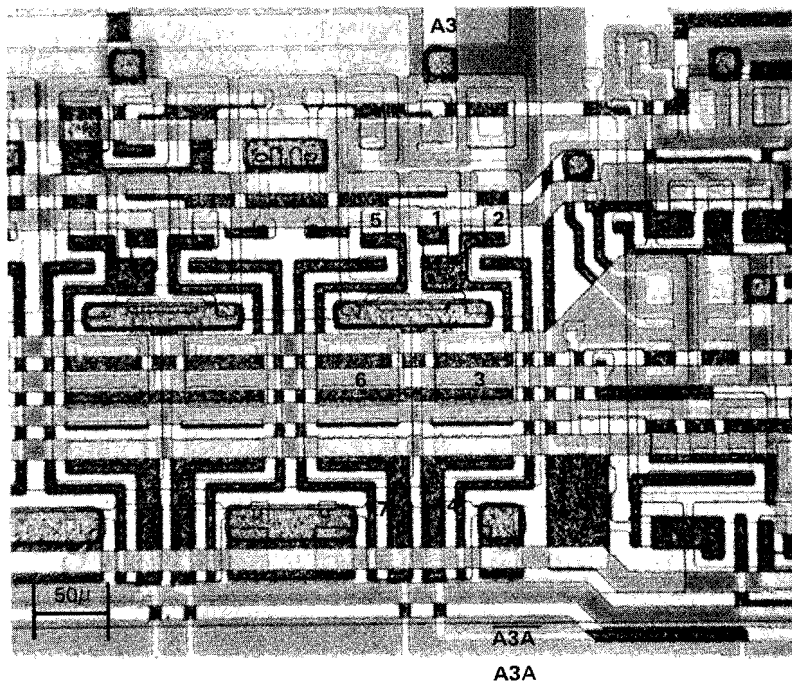


FIGURE 4-4. AMD Am2903 INPUT ADDRESS BUFFER A3
(INPUT ADDRESS BUFFERS B₀₋₃ AND INSTRUCTION INPUT BUFFERS ARE SIMILAR).

to the buffers used for the nine Instruction inputs. The difference is that the outputs of the Address buffers are connected to the top of the Schottky diode in the output stage. The outputs of the Instruction buffers are connected to the bottom of this Schottky diode. The Address buffers connect to the top of the diode to provide a voltage reference when the output is "low" for the decoder for the RAM cells. The decoder and the RAM cells will be discussed in paragraph 4-5.

The three-diode input is used on all of the I/O buffers. The three-diode input provides a higher threshold voltage and therefore greater noise immunity than if one diode were used. In order for the lower output transistor to be turned ON, node A must be three diode-drops above ground. This occurs when the input is about 1.4 volts or two diode-drops. Fast turn-off is aided by the Schottky diode. When the input is pulled "low" the Schottky diode will be turned ON and excess charge in the base of transistor 1 will be provided a low impedance discharge path.

4.3 - $\overline{\text{LSS}}$ and $\overline{\text{WRITE/MSS}}$ Input/Output Buffer.

When the $\overline{\text{LSS}}$ input is connected "low", the chip is programmed to operate as a Least-Significant-Slice (LSS). The logic diagram and schematic diagram in Figure 4-5 will show that this connection enables the buffer amplifier comprised of transistors 15, 16, 17 and 18 and disables NOR gate comprised of transistors 7 through 11. The $\overline{\text{WRITE}}$ output signal

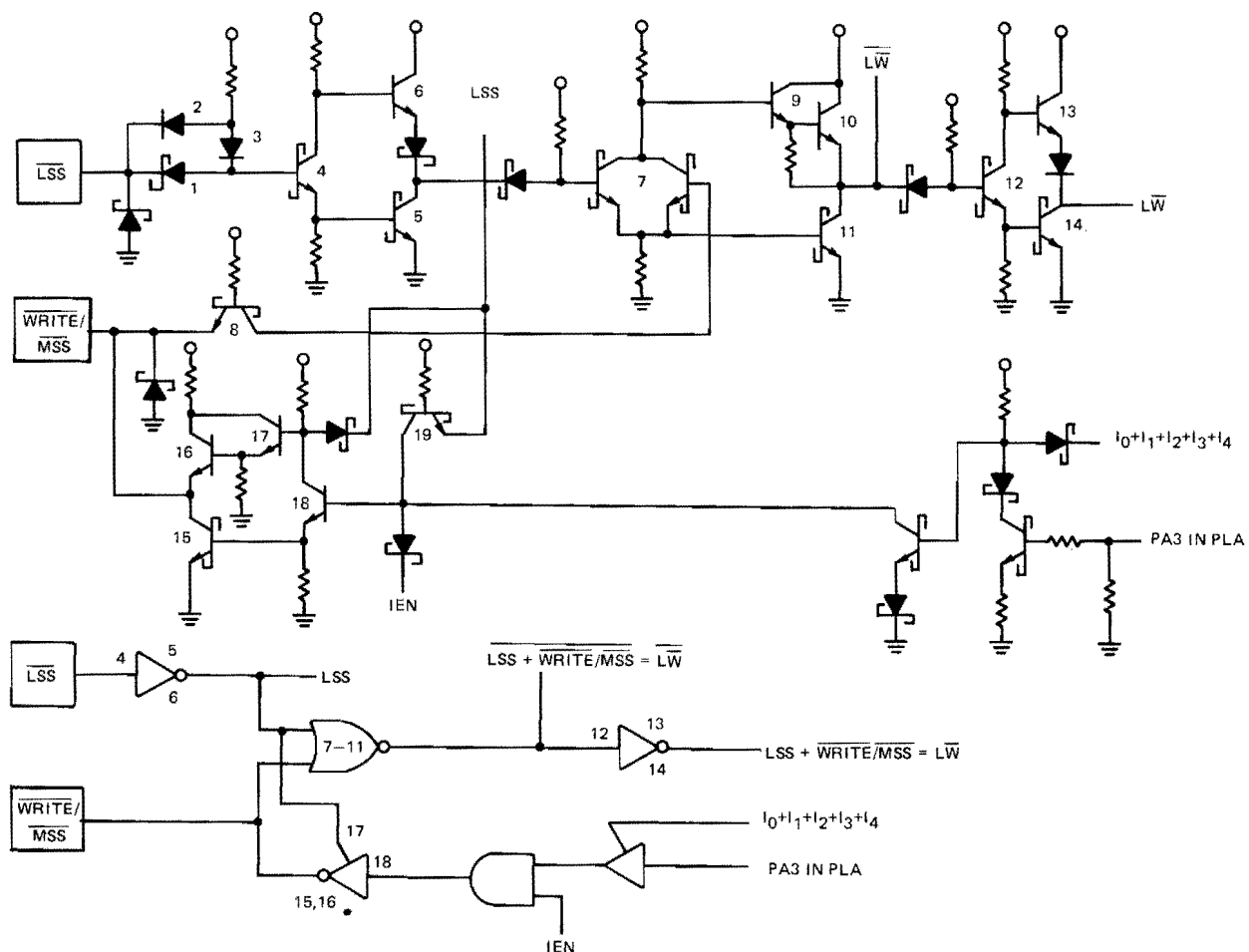
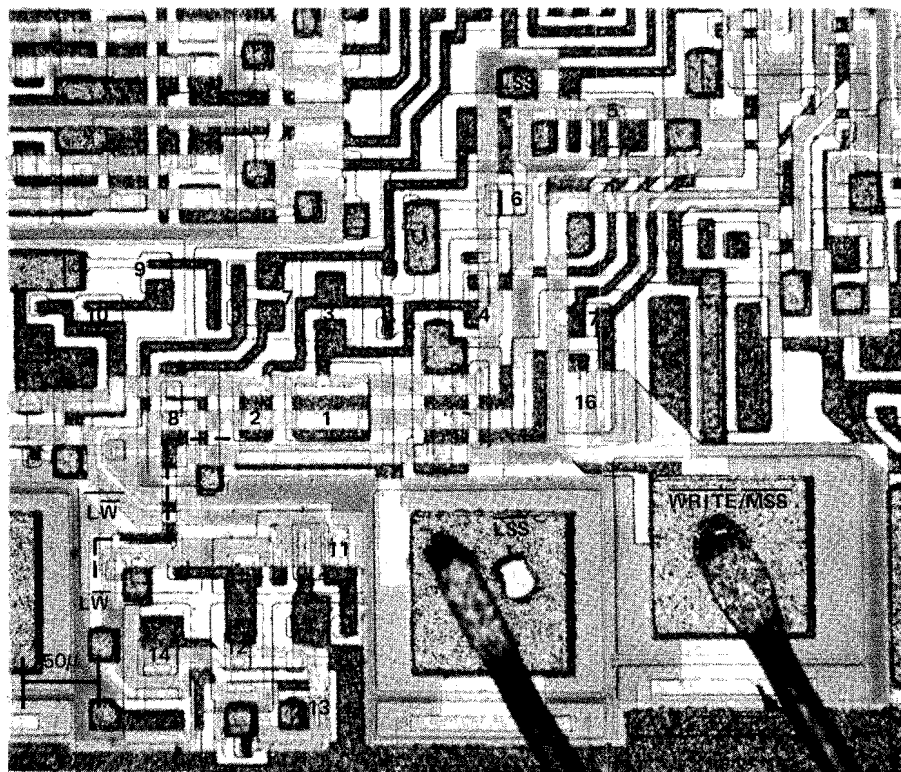


FIGURE 4-5. AMD Am2903: $\overline{LSS}$ AND $\overline{WRITE/MSS}$ INPUT/OUTPUT BUFFER.

is thus enabled onto the $\overline{\text{WRITE}}/\overline{\text{MSS}}$ bidirectional I/O pin.

When $\overline{\text{LSS}}$ is tied "high" the $\overline{\text{WRITE}}/\overline{\text{MSS}}$ pin becomes an input pin since the buffer amplifier will be disabled and the NOR-gate enabled. Connecting the $\overline{\text{WRITE}}/\overline{\text{MSS}}$ pin "high" causes the output of the NOR-gate to go "low" and programs the chip to operate as an Intermediate Slice (IS). Tying the $\overline{\text{WRITE}}/\overline{\text{MSS}}$ pin "low" programs the chip to operate as a Most-Significant-Slice (MSS).

4.4 - Data Bus Output Buffer DB_{0-3} .

The schematic diagram of the DB_0 output buffer is shown in Figure 4-6. The input buffer connected to this pin is shown in the MUX. The buffer is a standard TTL configuration with a darlington-connected transistor for the upper output device. A series-resistor is included for short circuit protection. Buffers that are not connected to external pins omit this series-resistor. The circuit has a tristate input (OEB) which causes the circuit to go into a high impedance state when it is pulled "low". When the circuit is enabled, data from the B output port of the RAM which has entered the Latch is connected to the input of the output buffer. This data is inverted by the buffer and presented to the DB_{0-3} output pins. This data is also available as an input to the MUX.

When the circuit is disabled by the tristate signal OEB , external data can be input to the MUX from the DB_{0-3} pins.

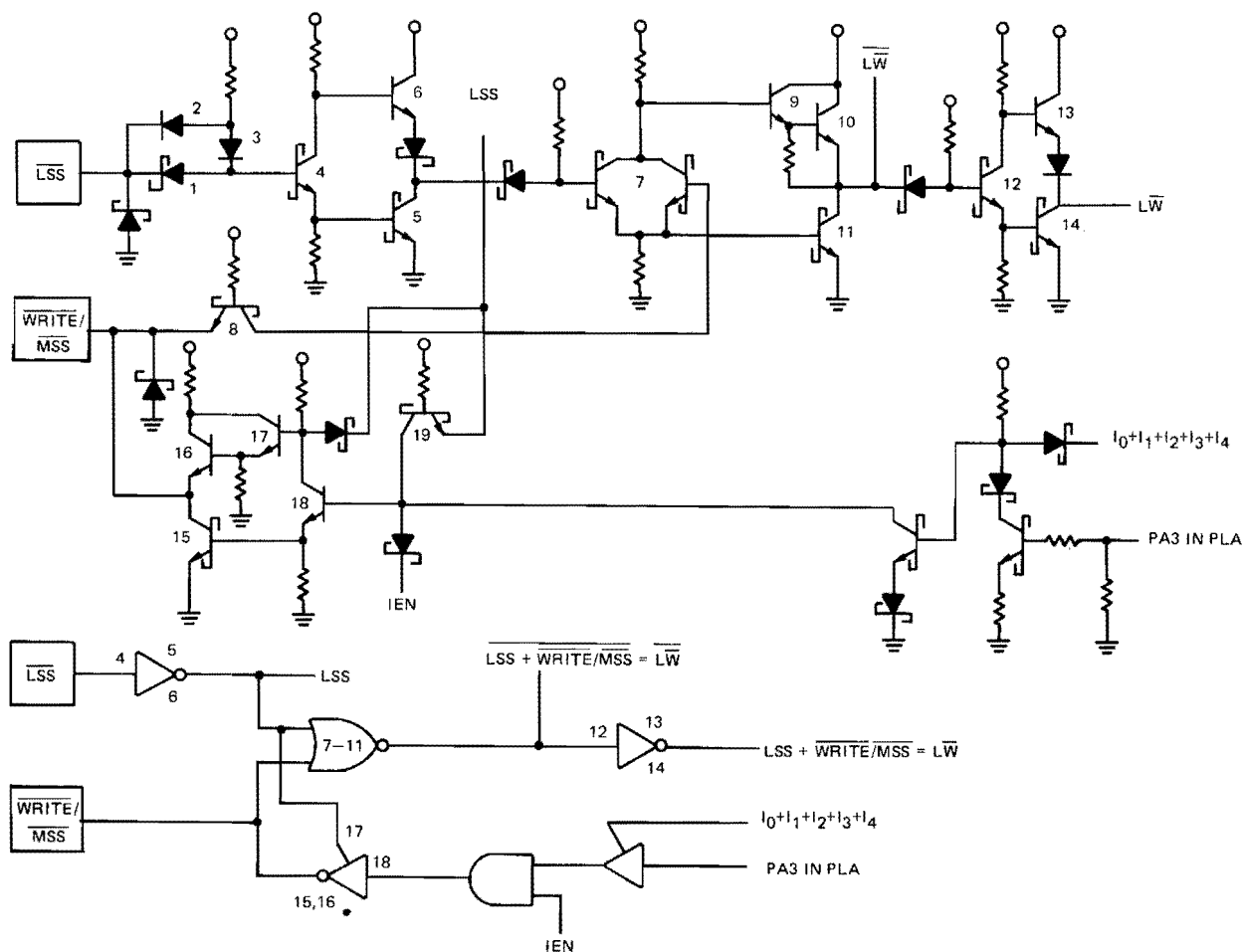
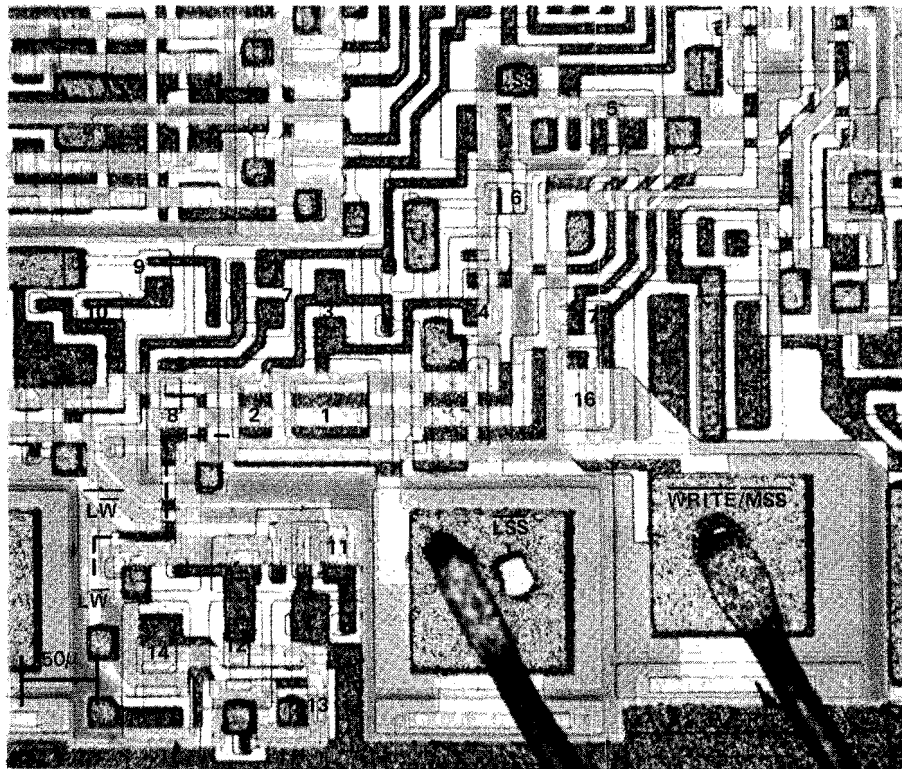


FIGURE 4-5. AMD Am2903: $\overline{LSS}$ AND $\overline{WRITE/MSS}$ INPUT/OUTPUT BUFFER.

is thus enabled onto the $\overline{\text{WRITE}}/\overline{\text{MSS}}$ bidirectional I/O pin.

When $\overline{\text{LSS}}$ is tied "high" the $\overline{\text{WRITE}}/\overline{\text{MSS}}$ pin becomes an input pin since the buffer amplifier will be disabled and the NOR-gate enabled. Connecting the $\overline{\text{WRITE}}/\overline{\text{MSS}}$ pin "high" causes the output of the NOR-gate to go "low" and programs the chip to operate as an Intermediate Slice (IS). Tying the $\overline{\text{WRITE}}/\overline{\text{MSS}}$ pin "low" programs the chip to operate as a Most-Significant-Slice (MSS).

4.4 - Data Bus Output Buffer DB_{0-3} .

The schematic diagram of the DB_0 output buffer is shown in Figure 4-6. The input buffer connected to this pin is shown in the MUX. The buffer is a standard TTL configuration with a darlington-connected transistor for the upper output device. A series-resistor is included for short circuit protection. Buffers that are not connected to external pins omit this series-resistor. The circuit has a tristate input (OE_B) which causes the circuit to go into a high impedance state when it is pulled "low". When the circuit is enabled, data from the B output port of the RAM which has entered the Latch is connected to the input of the output buffer. This data is inverted by the buffer and presented to the DB_{0-3} output pins. This data is also available as an input to the MUX.

When the circuit is disabled by the tristate signal OE_B , external data can be input to the MUX from the DB_{0-3} pins.

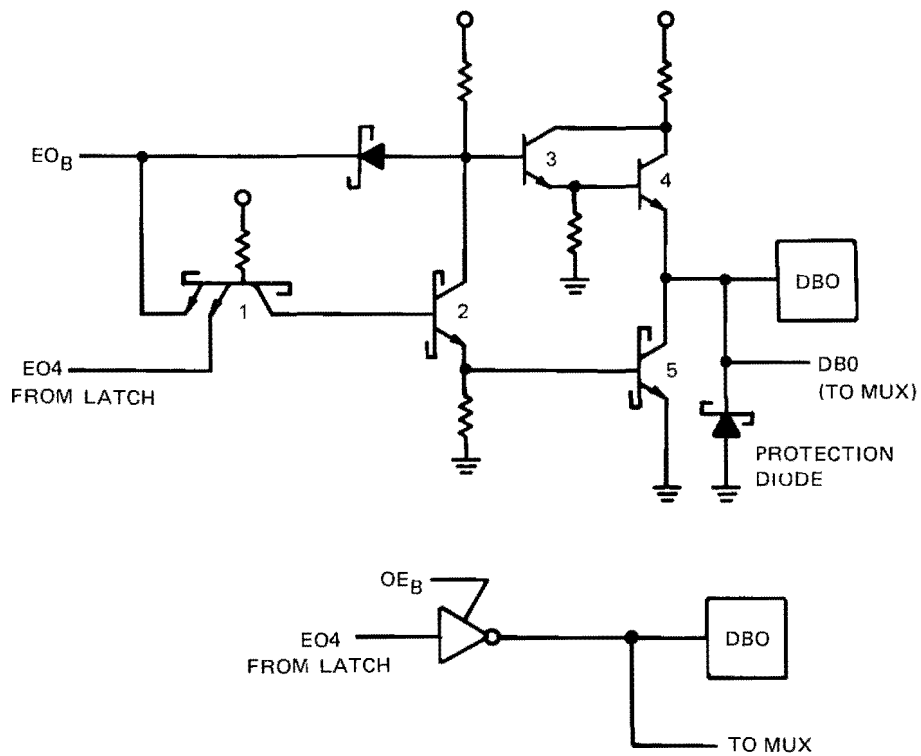
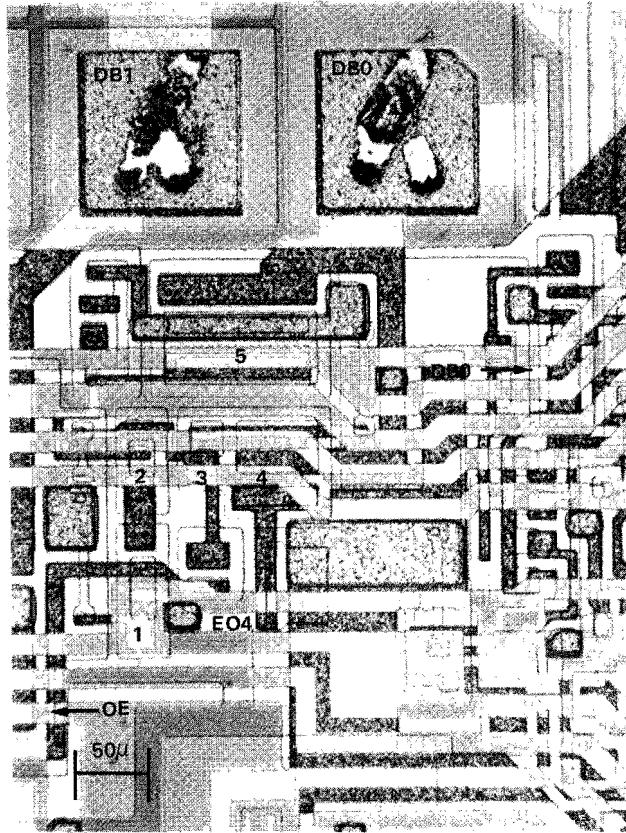


FIGURE 4-6. AMD Am2903 DB0 OUTPUT BUFFER.

4.5 - RAM Cell and Decoder

One of the 64 RAM cells is shown in Figure 4-7. Each of these RAM cells may be selected from either of two different address buses. READ and WRITE operations may be performed on cells selected from the B address bus and READ only may be performed on cells selected from the A address bus.

The RAM cell consists of cross-coupled transistors 3 and 4 and access transistors 1 and 2. When the cell is not selected, line A is a junction-diode-drop plus a Schottky-diode-drop above ground potential. Since very little current is flowing in the RAM cell, the voltage-drop across R1 connected to line C is probably considerably less than a diode-drop. Diode D1 therefore, is not conducting. The approximately one volt across the one cell is just sufficient to maintain the data in the cell.

Data is written into the cell when the cell is selected by the B address buffers. The selected B line is pulled "high" allowing data on lines E1 and E2 to be written into the cell. Data on lines E1 and E2 originate from the Y₀₋₃ inputs. Output data may be read from any cell addressed with either the A address buffers or the B address buffers. The data selected by the A address buffers is read out through transistors Q6 and data from the RAM cells addressed by the B address buffers are read out through transistors Q5.

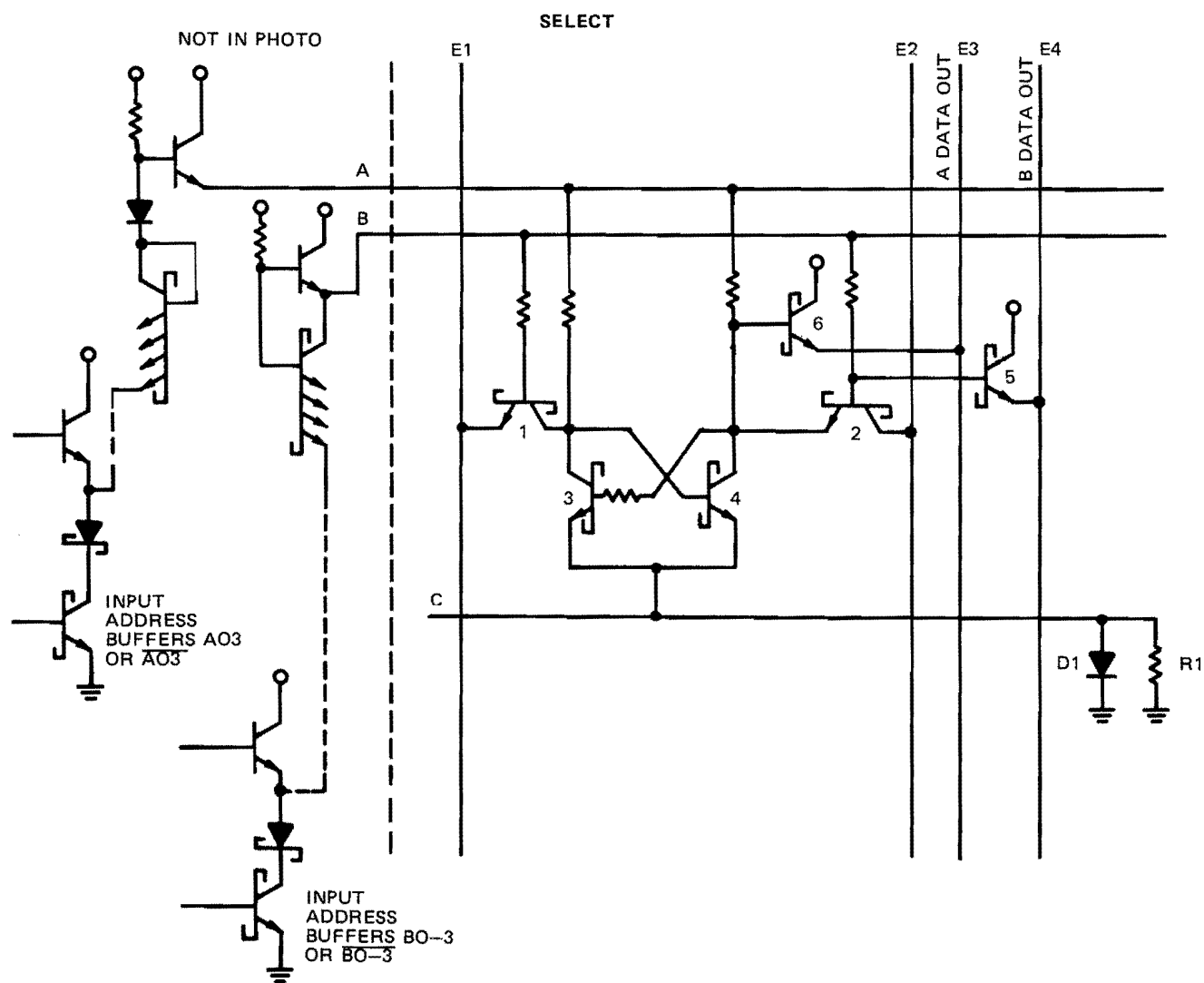
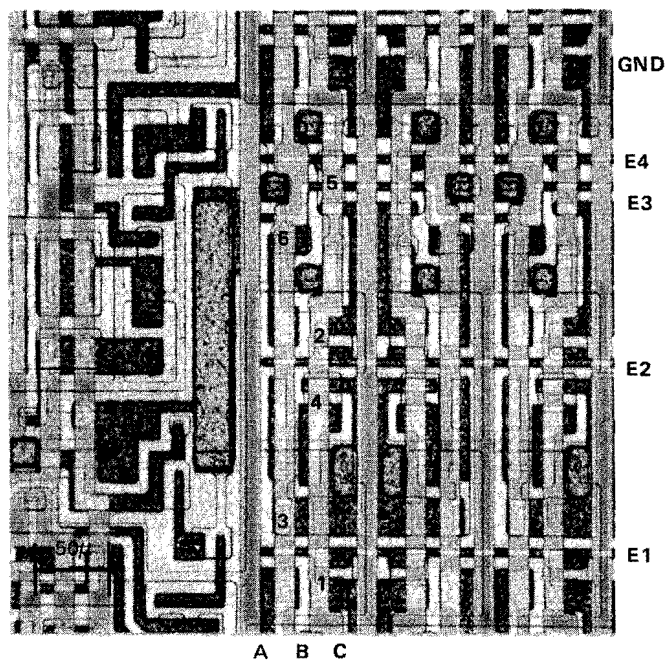


FIGURE 4-7. AMD Am2903 RAM CELL AND DECODER.

4.6 - Latch and Write Enable

The latch connects data from RAM output A and RAM output B to the MUX and to the DB output buffers. This Latch is transparent when the Clock input CP is "high" and holds the RAM output data when CP is "low". The schematic diagram and logic diagrams as well as the photo of this area of the circuit is shown in Figures 4-8 A and B. The latches for the A and B output of the RAM are the same except the Latch on the A output data passes the data through noninverted while the Latch on the B output data inverts the data. The reason of course is that the data from the B output gets inverted in the DB buffer before it is returned to the MUX.

The circuitry for the Write Enable is also shown in the photograph and the circuit schematic and logic schematic is shown at the bottom of Figure 4-8. Data is written into the RAM at the B address when the Write Enable input $\overline{WE}$ is "low" and the clock input CP is "low". If either the $\overline{WE}$ input or the clock CP is "high" both of the write signals E1 and E2 to the RAM cell will be "high".

4.7 - MUX

The MUX selects the inputs for the two ports of the ALU. Data to input port R is determined by control signal $\overline{EA}$. When $\overline{EA}$ is "high" the input is the inverted data found on the DA₀₋₃ inputs. When $\overline{EA}$ is "low", the data is the inverted data from the RAM A output ports. The

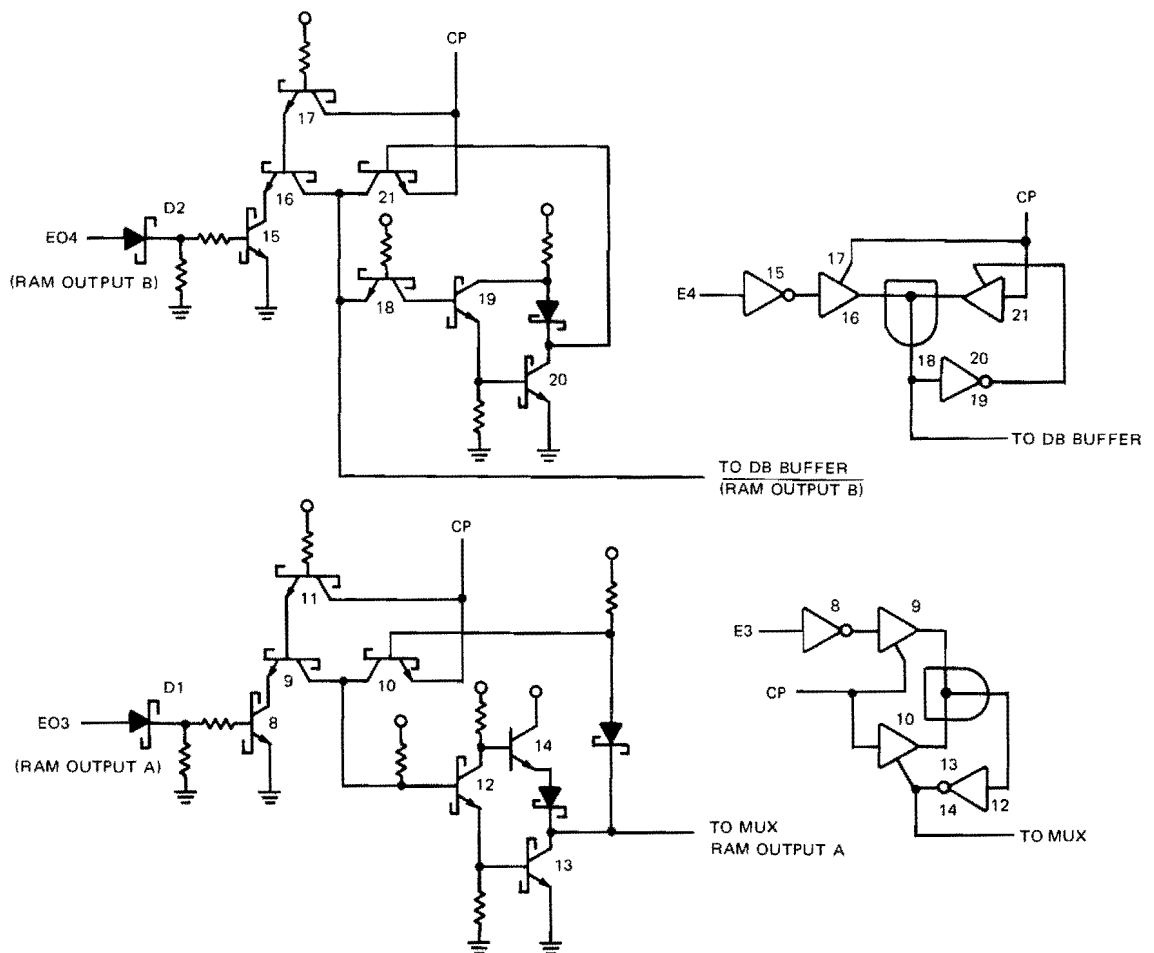
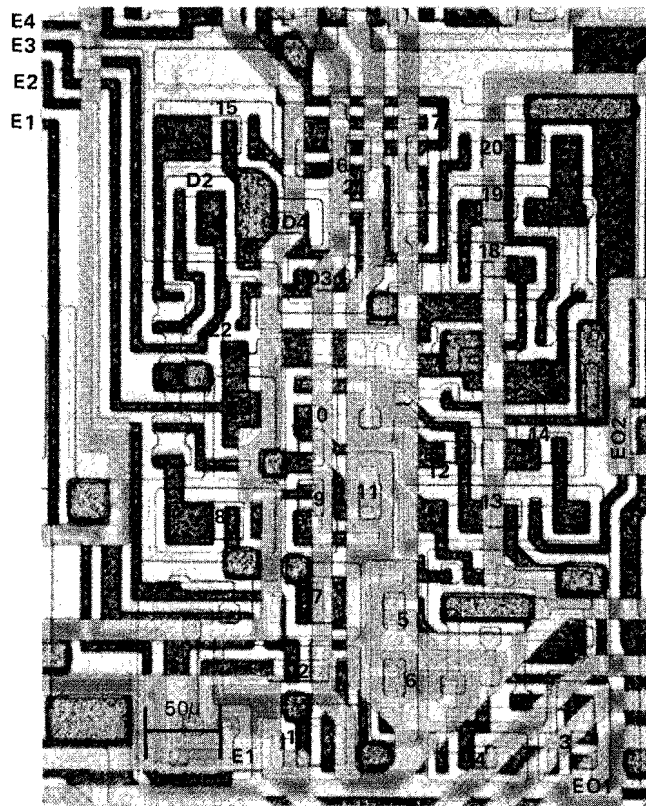


FIGURE 4-8A. AMD Am2903 LATCH AND WRITE ENABLE.

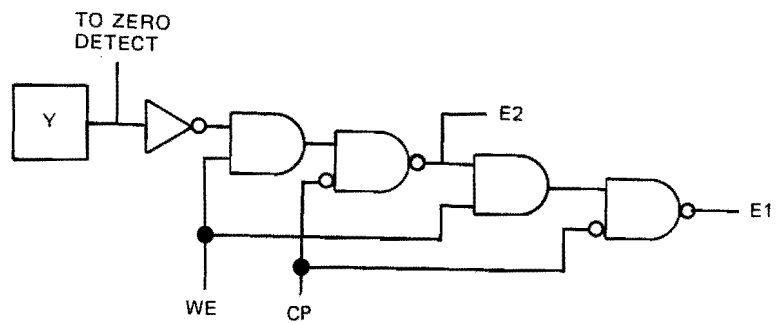
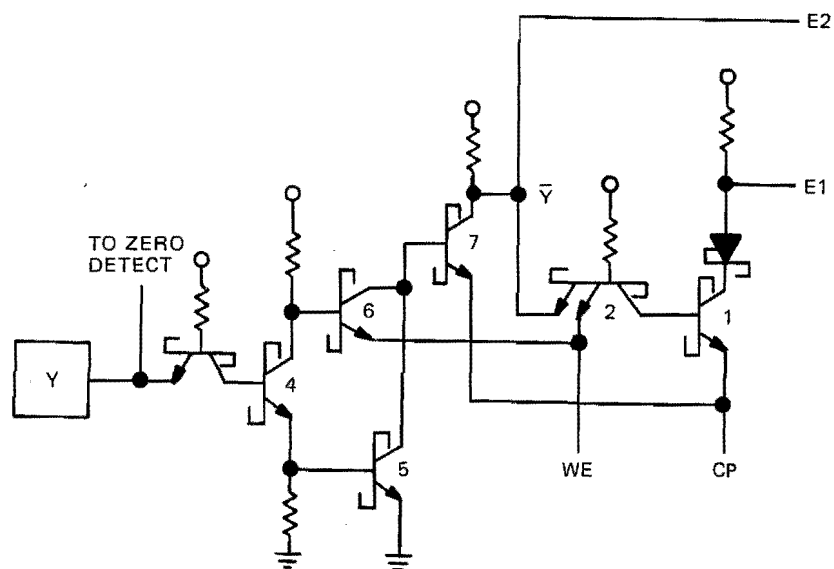


FIGURE 4-8B. AMD Am2903 LATCH AND WRITE ENABLE.

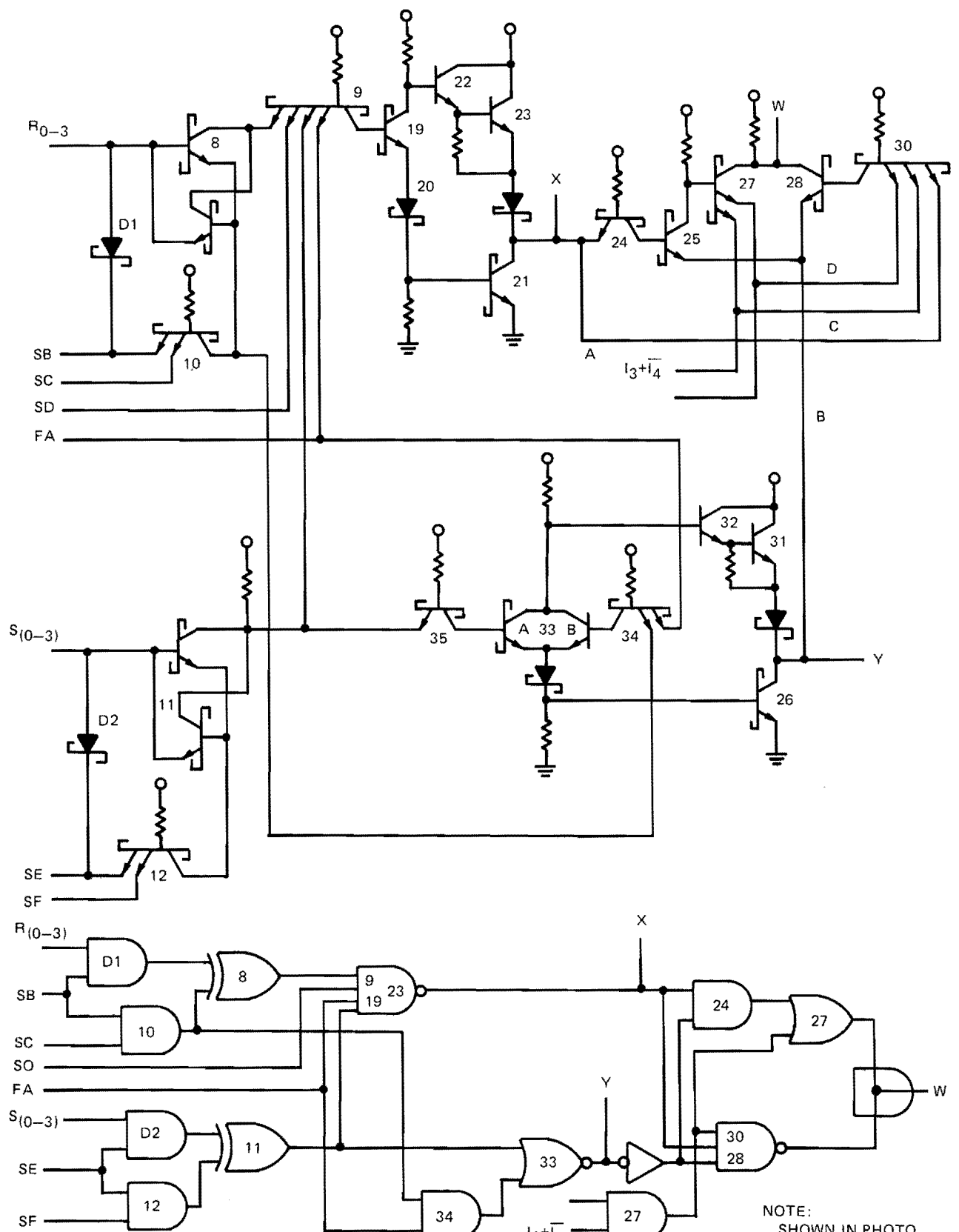
source of the data to the input of the ALU is controlled by the I_0 instruction input. The data comes from either the Q Register or the DB_0-3 inputs. The DB_0-3 inputs may in turn come from external data placed on the DB_0-3 input terminals or from the Latch as described in the previous paragraphs. The circuit configuration shown in Figure 4-9 makes efficient use of the components. It functions as a multiplexer combined with an Exclusive-OR circuit. The logic diagram representation and truth table are also shown.

4.8 - ALU

The ALU can perform seven arithmetic and nine logic operations on two four-bit operands. The MUX described previously selects the various pairs of operands from external and/or internal sources. The sixteen ALU functions are shown in Table 2 of the data sheet.

When the five instruction bits I_0-4 are "low", the Am2903 executes special functions. The nine special functions listed in Table 4 of the data sheet include multiply, divide and increment.

Complete analysis of the ALU is beyond the scope of this report, however, Figure 4-10 shows some of the ALU structure. The Boolean algebra expressions of the control signals that were traced out are shown on the diagram. The carry-in input C_N as well as the input signal from the Z terminal are combined in the SC control signal. The structure shown on Figure 4-10 which contains AND-gates, OR-gates and Exclusive-OR gates can provide all of the ALU functions listed in Table 2 of the data sheet.



$$SB = \overline{(I_0 + I_1 + I_2 + I_3 + I_4)}[(\overline{I_1} \cdot \overline{I_2} \cdot I_3) + (\overline{I_2} \cdot I_3 \cdot \overline{I_4})]$$

$$SC = \overline{CN + I_1(I_2 + I_3 + I_4) + Z[I_7 \cdot I_8(I_0 + I_1 + I_2 + I_3 + I_4)]}$$

FIGURE 4-10. AMD Am2903 ALU.

4.9 - The Q Shifter and Register

The Q Shifter and Register is shown in Figures 4-11 and 4-12. Figure 4-11 shows a single stage of the four-bit Q Register. This stage consists of a D flip-flop and an input-gating network to control the operation of the register. Figure 4-12 shows how the registers are interconnected and how the control signals into the input gating network causes the four bit register to shift up, shift down or hold. For the register to shift up, control signal GA is "high" and control signals GB and GC are "low". These control signals will disable the output buffer amplifier of QIO₀ and enable the buffer amplifier of QIO₃. A shift down operation is accomplished when control signal GB is "high" and GA and GC are "low". These signals will enable the buffer amplifier for QIO₀ and disable the buffer of QIO₃. The Q Register is loaded from the ALU when GC is "high" and GA and GB are "low". A hold is accomplished by ANDing the hold control signal with the Clock pulse before it is input to the Clock input of the D flip-flop. The output of each of the registers goes to the MUX. Control signals GA, GB, and HA come from the PLA to be described later.

4.11 - ALU Shifter and Y Outputs.

The ALU shifter consists of a multiplexer connected to the Y Output buffers. A schematic diagram and a photograph of a single stage as well as the logic diagram for all four stages is shown in Figures 4-13A and B.

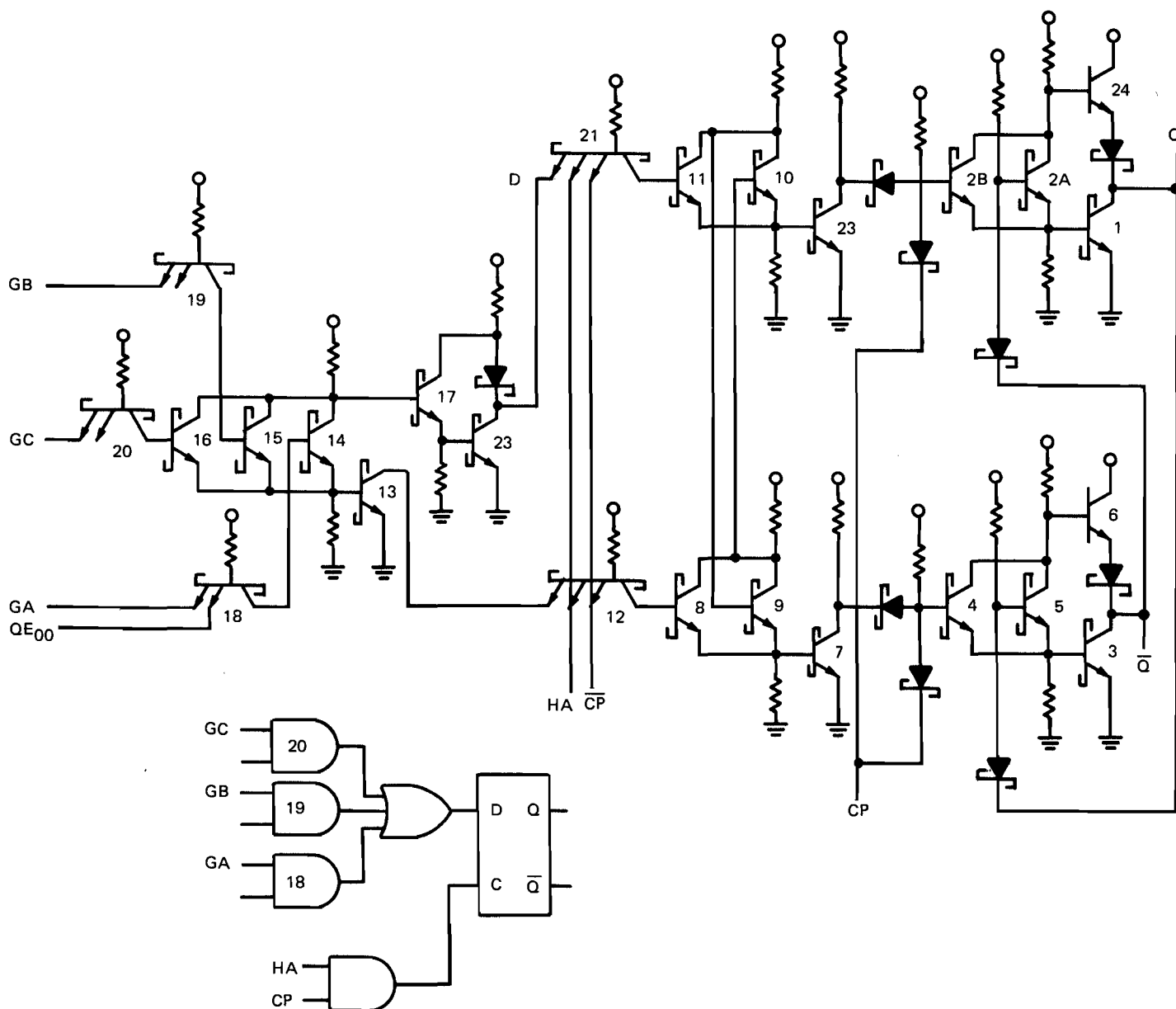
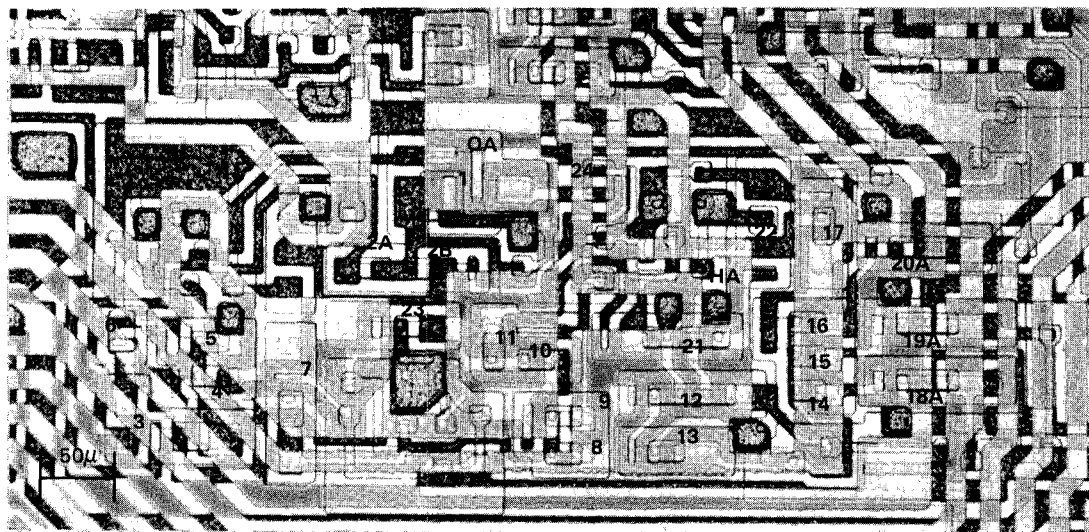


FIGURE 4-11. AMD Am2903 Q REGISTER SCHEMATIC AND LOGIC DIAGRAM.

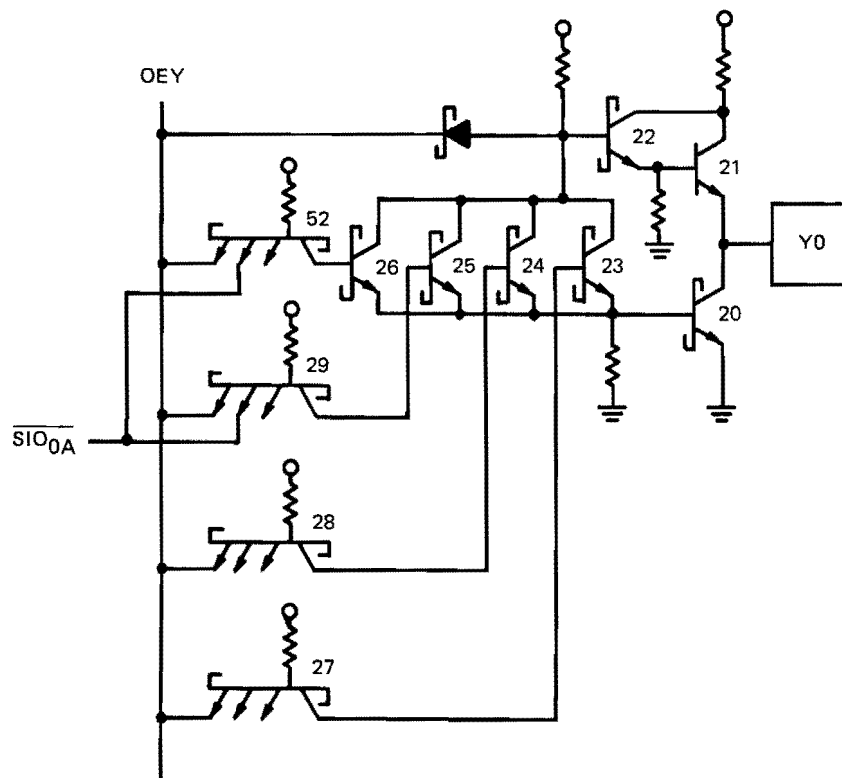
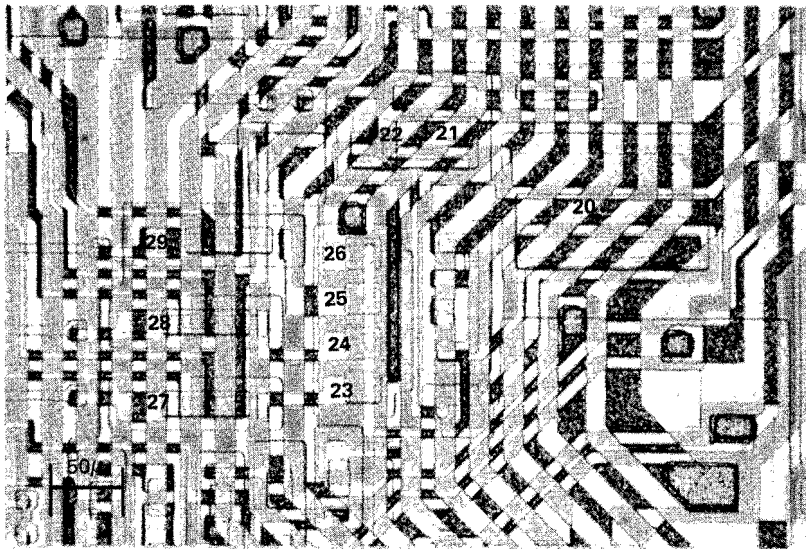


FIGURE 4-13A. AMD Am2903 ALU SHIFTER AND Y OUTPUTS.

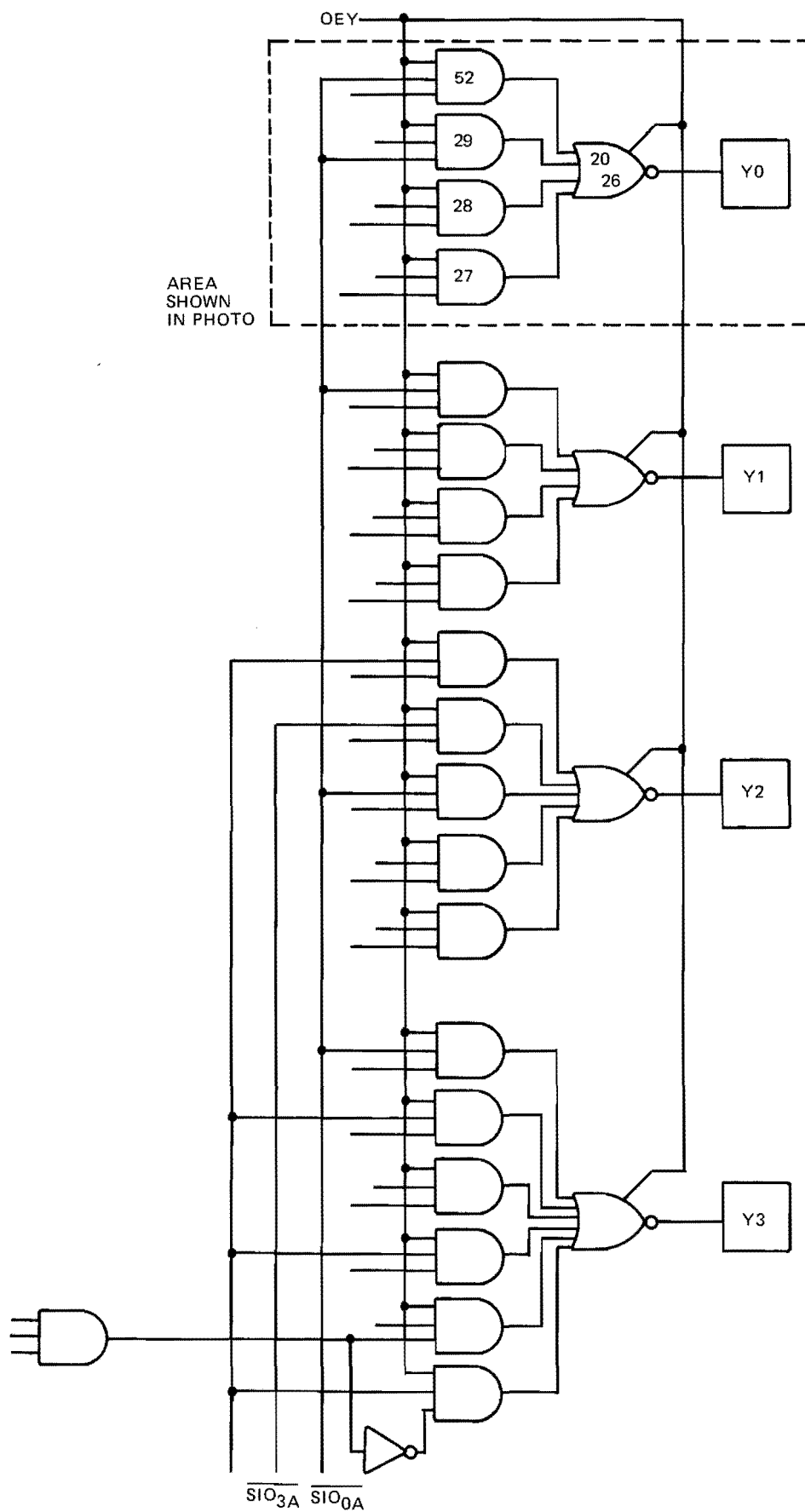


FIGURE 4-13B. AMD Am2903 ALU SHIFTER AND Y OUTPUTS.

Each stage consists of from four to six AND-gates which are connected to a NOR-gate which serves as the output buffer amplifier to the Y outputs. The Output Enable bus is connected to one input of each of the three input AND-gates and the upper output circuit of the output buffer. The output goes to a high impedance state when the Output Enable bus goes "low". The Output Enable amplifier is an inverting buffer, therefore the high impedance state of the Y buffers occurs when the $\overline{OE_Y}$ input pin is "high".

Table 3 in the data sheet shows the origin of the data which is output on the Y outputs for each of the sixteen instruction inputs. Besides the $\overline{OE_Y}$ signal only the $\overline{SI00A}$ and $\overline{SI03A}$ were traced. The $\overline{SI00A}$ signal goes to all four of the Y output stages. The $\overline{SI03A}$ signal goes to only Y2 and Y3. These connections correlate to the data shown in Table 3.

4.12 - $SI0_0$ and $SI0_3$ Functions.

The functional block diagram, Figure 4-1, show $SI0_0$ and $SI0_3$ as inputs and outputs of the ALU Shifter. Table 3 and 4 in the data sheet show that these two terminals perform many more functions than is indicated by the block diagram. As the functional diagram indicates, the ALU outputs F0 to F3 may be obtained from either $SI0_0$ or $SI0_3$ output terminals and the $SI0_0$ and $SI0_3$ terminals may serve as inputs to transfer data to the Y_{0-3} outputs. Tables 3 and 4 in the Data Sheet also show that in addition to these functions, parity for the F0, F1, F2, F3, ALU outputs and the $SI0_3$ input may be obtained at the $SI0_0$ output. Also the Exclusive-OR

function of the R3 output of MUX and F3 output of ALU may be obtained at the $SI0_3$ output. The schematic diagram and logic diagram showing how these functions are obtained is shown in Figures 4-14 A and B.

Two different types of Exclusive-OR circuits are used on the $\Lambda m2903$ chip. Both types are used in the parity circuit shown in Figures 4-14 A and B. One configuration of the Exclusive-OR circuit is formed by transistors 1, 2 and 3. This same configuration is used by transistors 8, 9 and 10. A second configuration is formed by transistors 12, 13, 14 and 15, also 11, 16, 17, and 18. The advantages of one configuration over the other are not immediately obvious.

The Instruction input I_8 will cause the output buffer driving terminal $SI0_3$ to go to a high impedance state when it is pulled "low". Likewise when $\overline{I_8}$ is "high" (I_8 is "low") the output buffer driving the $SI0_0$ terminal will be placed in a high impedance state. This corresponds to Tables 3 and 4 which shows that when I_8 is "low", the $SI0_3$ terminal acts as either an input or is in the high impedance state. Likewise when I_8 is "high" $SI0_0$ terminal acts as either an input or is in the high impedance state.

4.13 - Z Output

The circuitry showing the Z output function is shown in Figure 4-15. The Zero, Z, pin is an open-collector input/output that can be wire-ORed between slices. This figure shows that the Z output is a large multiplexer with nine different inputs. Four of the inputs are $Y0_3$ and these inputs may be logically summed together.

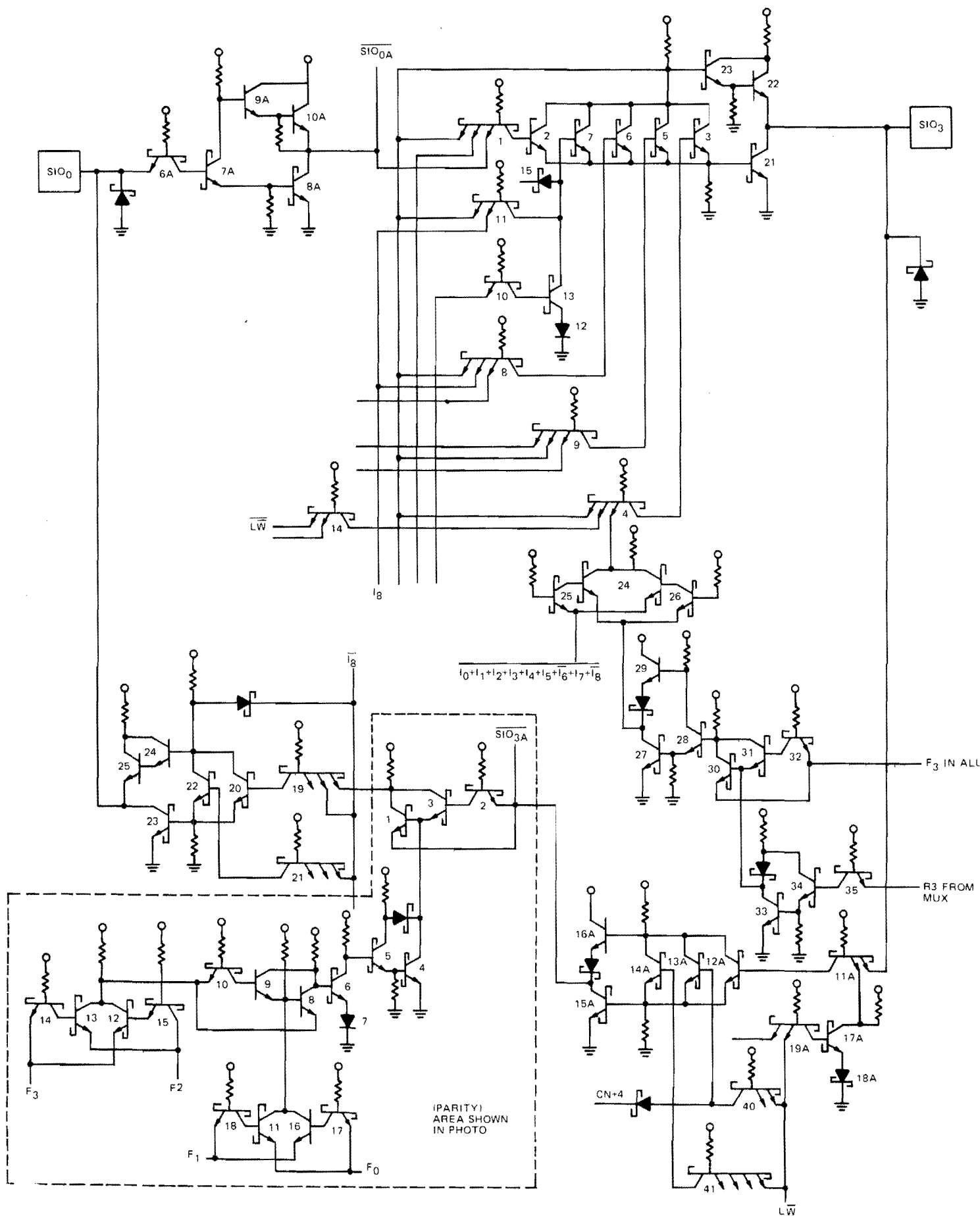


FIGURE 4-14A. AMD Am2903 SIO₀ AND SIO₃ FUNCTIONS SCHEMATIC DIAGRAM.

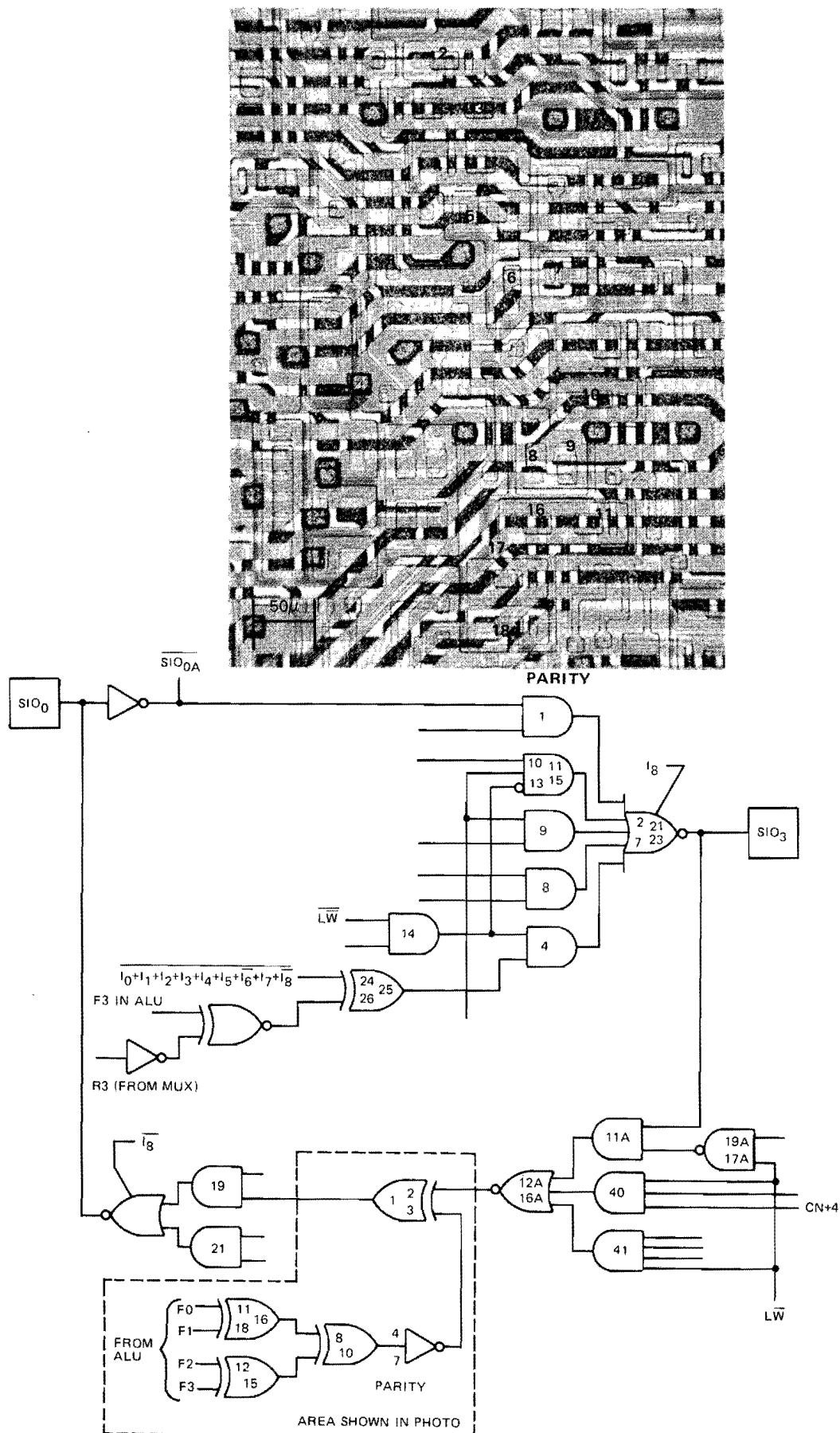


FIGURE 4-14B. AMD Am2903 LOGIC DIAGRAM OF SIO_0 AND SIO_3 FUNCTIONS.

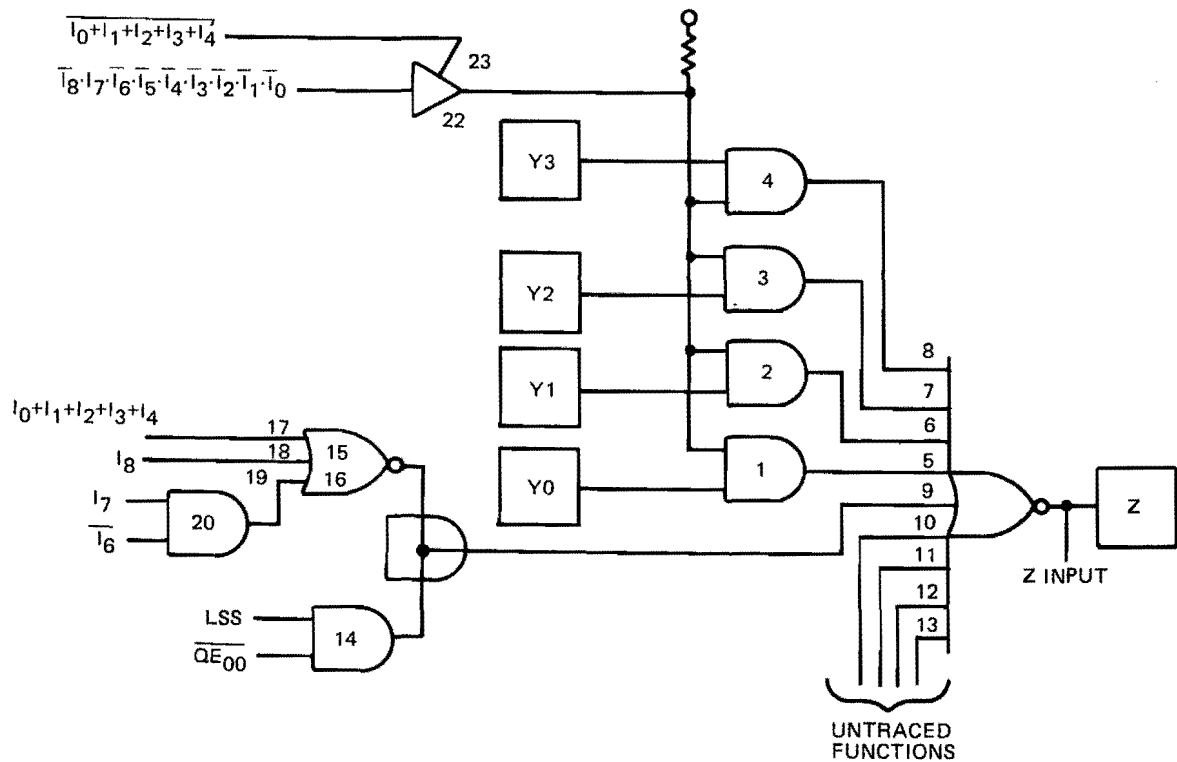
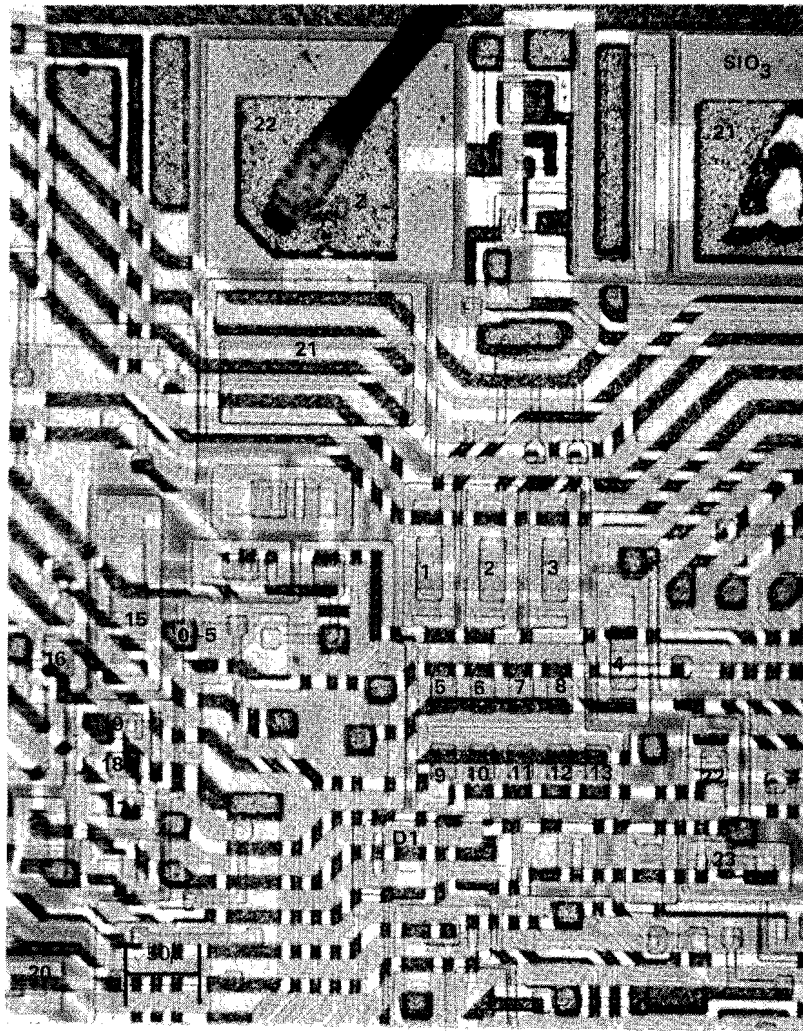


FIGURE 4-15A. AMD Am2903 Z INPUT/OUTPUT FUNCTIONS.

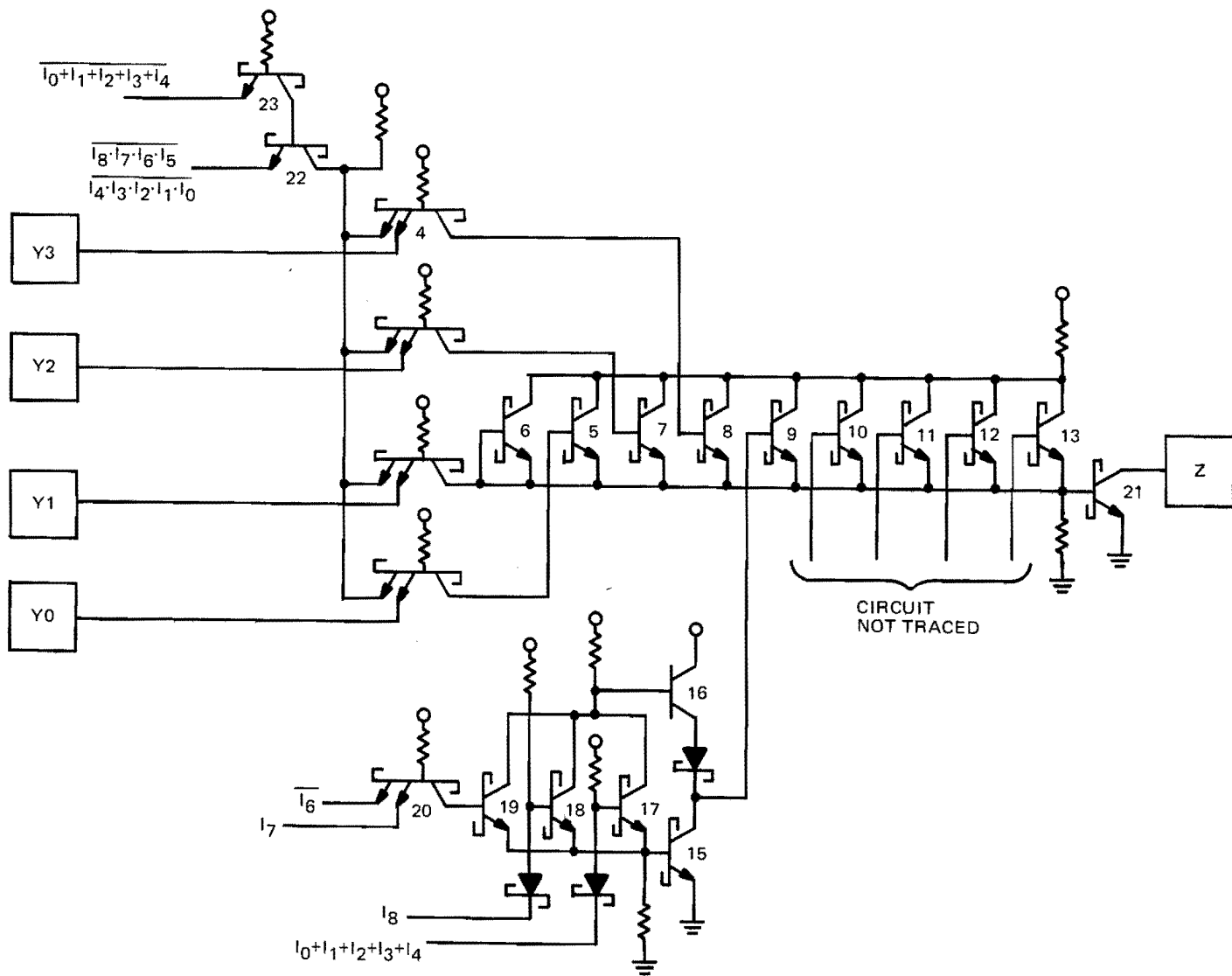


FIGURE 4-15B. AMD Am2903 Z INPUT/OUTPUT FUNCTIONS.

Figure 5 in the data sheet shows the function of the Z terminal when the chip is wired as the Most-Significant-Slice, Intermediate-Slice or Least-Significant-Slice. This table shows the other inputs to the multiplexer include the S3 input from the MUX, the logically summed outputs of the Q register, the logically summed outputs of the Q register and the ALU, or they provide the results of a sign compare when connected as the Most-Significant-Slice. If none of the inputs to the multiplexer are selected, the Z terminal serves as an input to the Instruction decode circuitry.

4.14 - Instruction PLA

The nine Instruction inputs of the Am2903 chip are decoded with both random logic and a programmed logic array (PLA structure). All of the sixteen instructions derived from Instruction inputs I_{0-4} that control the ALU operations shown in Table 2 of the Data Sheet, are decoded with random logic. The nine special functions derived from Instruction inputs I_{5-8} shown in table 4 of the data sheet are also decoded by random logic. A PLA structure however, is used to decode the sixteen instructions shown in Table 3 of the data sheet. The PLA and logic diagram are shown in Figure 4-16.

The PLA is represented in symbolic form in this figure. The right-hand side of the figure functions as fourteen AND-gates. Each gate is represented by one of the horizontal lines. These lines are metal buses which overlay islands of lightly doped N-type silicon. Schottky-

diodes are formed between the metal bus and the silicon islands by placing contact openings in the appropriate places. The vertical lines on the right-hand side of Figure 4-16A indicate the silicon islands and the circles at the intersection of the horizontal and vertical lines indicate the location of Schottky diodes. Instruction inputs I_{5-8} and their complements are connected to the silicon islands. Control signal $\overline{LW}$ and its complement are also connected to the islands.

The schematic representation at the bottom of the figure shows that if any of the Schottky diodes to which the metal line is attached are pulled "low" the metal line will be pulled "low". All of the Schottky diodes have to be "high" for the metal line to be "high". Each line thus functions as an AND-gate and is "high" only when addressed by the proper hexadecimal code. The hex-code for the individual lines are shown on the right-hand side of the PLA structure.

The left-hand side of Figure 4-16A represents the connection of the multiple-emitter transistors. Each circle on the left-hand side on the horizontal line represents an emitter. The vertical lines show the interconnections of these emitters. The vertical lines will be "low" if all of the emitters to which they are connected are "low". If any one of the emitters is "high", the vertical line to which it is connected will be "high". The left-hand side of the PLA thus functions as OR-gates. The outputs of the PLA will be "low" unless one of the horizontal lines to which it is connected is addressed by the proper hex-code.

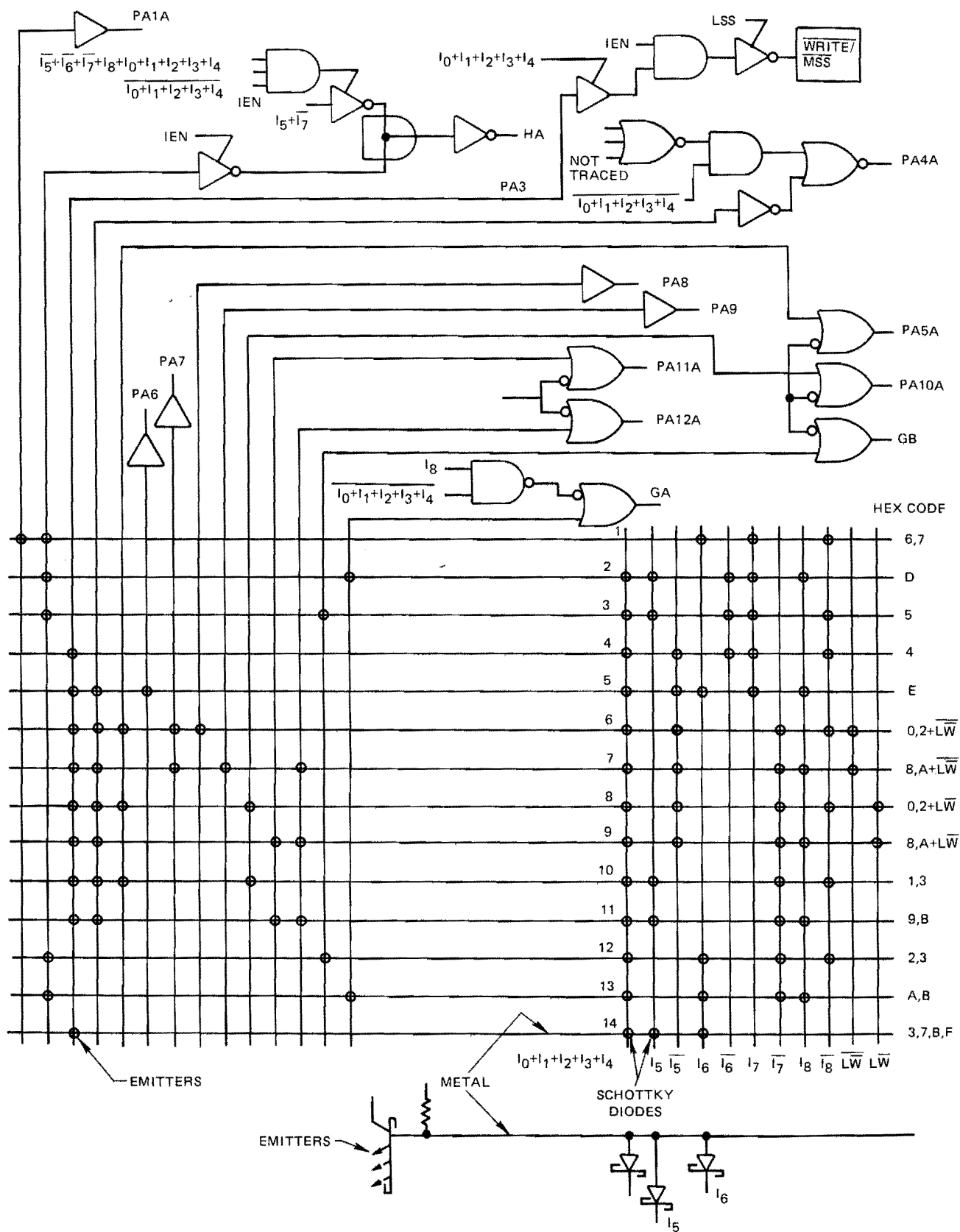


FIGURE 4-16A. AMD Am2903 INSTRUCTION PLA FOR I_5 , I_6 , I_7 , I_8 .

Figure 4-16A shows the logic diagram of other circuitry which was traced from the chip. Some of the control signals generated by this logic is referred to in some of the preceding paragraphs. Other signals were not traced to their destination.

Operation of this PLA may be checked by tracing signal PA3 which goes to the $\overline{\text{Write}}/\overline{\text{MSS}}$ output pad. This output line is "high" except for instructions 5, 6, C and D. This signal is inverted before it gets to the output pad. Table 3 of the Data Sheet shows that the $\overline{\text{Write}}$ output signal is "high" only for these four instructions.

This PLA structure does not provide any of the decoding for special functions in Table 4 of the Data Sheet, since this table is valid only if I_{0-4} are "low". This condition would cause all of the outputs from the PLA to be "low" regardless of the condition of the other instruction inputs.

SECTION V - SPECIFICATIONS REVIEW

The specifications review is based on Publication Am-PUB074 which was copyrighted by Advanced Micro Devices Inc. in 1978. No absolute maximum ratings were found in this publication.

DC Characteristics

DC characteristics over the specified temperature and voltage operating range is given for both the commercial-temperature range and MIL-temperature range units. The commercial circuits are specified over a temperature range of 0 to 70°C and a power supply voltage of $5V \pm 5\%$. The MIL-range circuits are specified over a temperature range of -55 to +125°C and a voltage of $5V \pm 10\%$.

The Output-High-Voltage, V_{OH} , is given as 2.4 volts minimum which is the standard TTL specification. The source current at all of the outputs except for Y_{0-3} and $\overline{G}/N$ at this output voltage is -800uA. The source current for the Y_{0-3} and $\overline{G}/N$ outputs is 1.6 mA. No distinctions are made between the commercial- and MIL-grade circuits.

The Z output is an open-collector output, thus the V_{OH} parameter cannot be measured directly. An output current I_{CEX} is measured instead. The specification is .25 mA max with V_{CC} equal to its minimum value and the Z output pad raised

to 5.5 volts. This current is caused primarily by the input circuitry connected to this pin rather than output leakage current.

The output "low" voltage, V_{OL} , is divided into five categories for the different output pins. Two of these categories are also subdivided into commercial-grade and MIL-grade circuits. All of these categories have the same V_{OL} voltage specification of 0.5 volts but each category uses a different sink current. The Y_{0-3} and the Z outputs have the highest current rating. The specified sink current I_{OL} is 20 mA for the commercial-grade circuits and 16 mA for the MIL-grade circuits. The lower current for the MIL-grade circuits reflect the higher collector saturation resistance at the higher operating temperature limit.

The lowest sink current is specified for the $C_N + 4$ output, the two SIO outputs, the two QIO outputs and the Write output. This sink current is 8 mA. No distinction is made between the commercial-grade and MIL-grade circuits, probably because this specification is easily met even at 125°C.

The Input-High level V_{IH} specification of 2 volts and the Input-"Low" level V_{IL} specification of 0.8 volts is standard for TTL circuits. Since the V_{OH} and V_{OL} specifications guarantee an output-"high" voltage of 2.4 volts and an output low voltage of 0.5 volts respectively the worst case noise margin for a "1" input is 400 mV and the worst case noise margin for a "0" input is 300 mV.

The Input-low current I_{IL} is divided into four categories for the different input terminals. The measurement is made with an input voltage held at 0.5 volts with V_{CC} at its maximum voltage. The specified currents are the currents that flow out of the input terminal and into the output terminal to which it is connected. The current specified range from 0.36 mA to 2.5 mA max. The minus sign which indicates current is flowing out of the test circuit is missing in this specification.

The input "high" current I_{IH} is divided into five different categories. This current is measured with the input voltage at 2.7 volts and the V_{CC} voltage at its maximum value. The input "high" current ranges from 20 mA to 120 mA. The category containing the C_N input specification and the category containing the Y_{0-3} input current specification could be easily combined since the specifications for these two categories differ by less than 10%.

The currents of the tristate outputs when in the High-Impedance state, are specified by the I_{OZH} and the I_{OZL} specifications. These outputs are divided into two categories with Y_{0-3} in one category and the remaining tristate outputs in the second category. Each category is measured when the output voltage is pulled "high" and when it is "low". These specifications are determined primarily by the input circuitry connected to these pins and not the tristate outputs. For the Y outputs $I_{OZH} = I_{IN}$ and I_{OZL} is slightly greater than I_{IL} .

The specifications for the power supply current I_{CC} shows that the current is temperature dependent. Maximum current specifications are given for 25°C, 70°C and 125°C. The current specification increases from 258 milliamps at 125°C to 335 milliamps at 25°C. Other specifications are given for a temperature range of 0° to 70° and -55° to +125°C. The specifications for these temperature ranges are in reality the specification at the lowest temperature in the range. A maximum current drain of 395 milliamps at -55°C can be expected.

Switching Characteristics

Three different tables are provided to define the timing characteristics of the Am2903. All of these tables however, provide only typical or nominal timing characteristics at 25°C and 5 volts.

Table 1 shows the Write pulse and Clock characteristics. Table 2 shows the combinational propagation delays between the various inputs to the appropriate outputs. Table 3 shows the setup and hold times required between the input signal and the Clock pulse. The one exception to this statement is when data is written into the Register addressed by the B address. The setup time in this case is between the B address and when the clock and $\overline{WE}$ terminal are both "low".

In summary the DC characteristics are adequately specified. The switching characteristics need to include max and min values over the operating temperature and voltage ranges. AMD reports that these are now available.

SECTION VI - CONCLUSIONS

Analysis of the Am2903 four-bit expandable microprocessor slice found it to be a very useful and versatile LSI circuit with features that will help reduce chip count and increase the speed of bit-slice systems. Sophisticated processing techniques such as double-level metal, Schottky-Diode-Clamped transistors, and washed-emitters were used to increase the speed of the circuit and reduce the die size. All of these processes appeared to be in good control and are not expected to detract from the reliability of the device. The reliability of this and similar products made with this process should, however, be proven since these advanced processing techniques may demonstrate new failure mechanisms.*

Two abnormalities were found during the external package analysis. The first problem is an uncommon one and consists of a bad braze between pin 11 and the side-brazed package. On one unit the pin was missing and on another commercial unit a poor braze was observed on the same pin location. The second abnormality, discovered during X-ray, consists of a poor die attach. Over 50% of the die attach area of this mil-temperature-range part was void. A good die attach is fairly important for this part since the chip dissipation may be as high as 2.2 watts. Other areas that were tested such as the gas analysis and wire strength tests were found to exceed MIL-STD-883 requirements.

* AMD reports that this process is the same as used by the 2901A four-bit slice (39510/440) which has proven reliability.

SECTION VII - RECOMMENDATIONS

We recommend that the following be investigated further or monitored to help alleviate any reliability problems.

The die attach area of this relatively large bipolar chip was found to have large voids. A good die attach is important to obtain good thermal conductivity between the chip and the package. The large 48-pin ceramic package will serve as a good heat sink if a good die attach is obtained. A poor die attach will cause excessive heating of the chip as well as possible stresses which may result in microcracks or even cracking of the die.

The maximum and/or minimum switching characteristics must also be provided over the temperature and voltage ranges.

Am2903

The Superslice™

INCLUDES PRELIMINARY SWITCHING DATA

DISTINCTIVE CHARACTERISTICS

- **Expandable Register File—**
Like the Am2901A, the Am2903 contains 16 internal working registers arranged in a two-address architecture. But the Am2903 includes the necessary "hooks" to expand the register file externally to any number of registers.
- **Built-in Multiplication Logic—**
Performing multiplication with the Am2901A requires a few external gates--these gates are contained on-chip in the Am2903. Three special instructions are used for unsigned multiplication, two's complement multiplication, and the last cycle of a two's complement multiplication.
- **Built-in Division Logic—**
The Am2903 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- **Built-in Normalization Logic—**
The Am2903 can simultaneously shift the Q Register and count in a working register. Thus, the mantissa and exponent of a floating point number can be developed using a single microcycle per shift. Status flags indicate when the operation is complete.
- **Built-in Parity Generation Circuitry—**
The Am2903 can supply parity across the entire ALU output for use in error detection and CRC code generation.
- **Built-in Sign Extension Circuitry—**
To facilitate operation on different length two's complement numbers, the Am2903 provides the capability to extend the sign at any slice boundary.

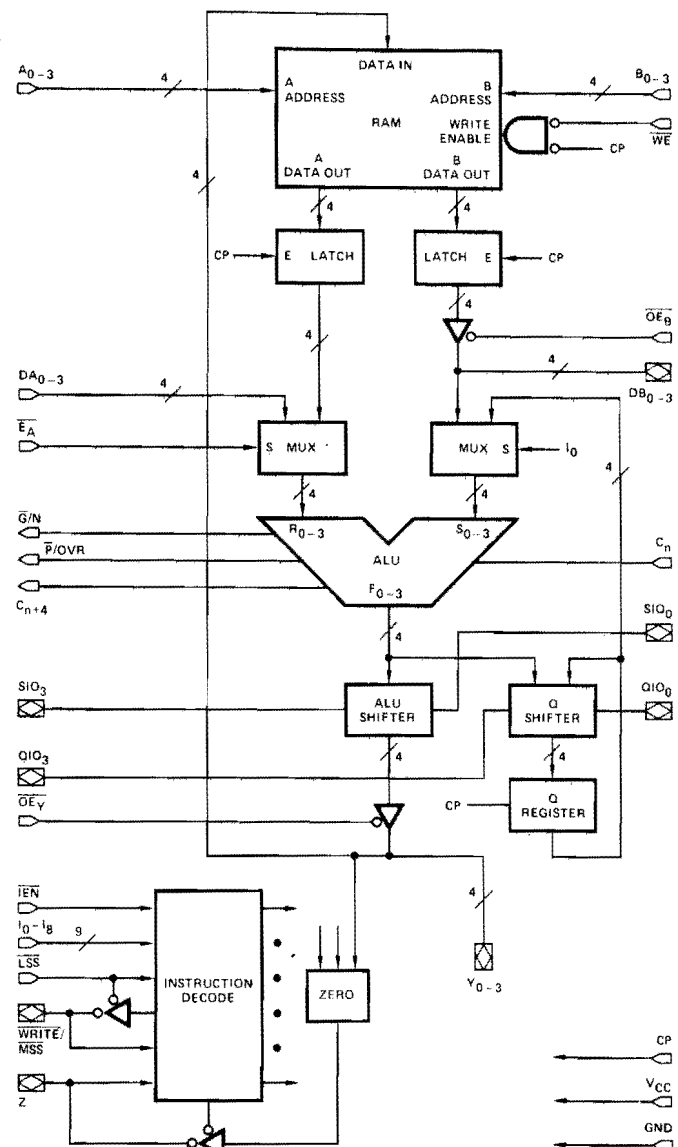
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GENERAL DESCRIPTION

The Am2903 is a four-bit expandable bipolar microprocessor slice. The Am2903 performs all functions performed by the industry standard Am2901A and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am2903. In addition to its complete arithmetic and logic instruction set, the Am2903 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The Am2903 is supplied in a 48 pin dual in-line package.

BLOCK DIAGRAM



ARCHITECTURE OF THE Am2903

The Am2903 is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPU's, peripheral controllers, microprogrammable machines, and numerous other applications. The microinstruction flexibility of the Am2903 allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function, and destination. The Am2903 is cascadable with full lookahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OE}_B$ three-state output enable, RAM data can be read directly at the Am2903 DB I/O port.

External data at the Am2903 Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am2903 high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{E}_A$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OE}_B$ and I_0 inputs select RAM output port B, DB external data input, or the Q Register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am2903 ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table 1 shows all possible pairs of ALU operands as a function of the $\overline{E}_A$, $\overline{OE}_B$, and I_0 inputs.

When instruction bits I_4 , I_3 , I_2 , I_1 , and I_0 are LOW, the Am2903 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am2903 executes instructions other than the nine special functions, the ALU operation is determined by instruction bits I_4 , I_3 , I_2 , and I_1 . Table 2 defines the ALU operation as a function of these four instruction bits.

Am2903's may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am2903's are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals required for a lookahead carry scheme are generated by the Am2903 and are available as outputs of the least significant and intermediate slices.

The Am2903 also generates a carry-out signal, C_{n+4} , which is generally available as an output of each slice. Both the carry-in, C_n , and carry-out, C_{n+4} , signals are active HIGH. The ALU

TABLE 1. ALU OPERAND SOURCES

$\overline{E}_A$	I_0	$\overline{OE}_B$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB ₀₋₃
L	H	X	RAM Output A	Q Register
H	L	L	DA ₀₋₃	RAM Output B
H	L	H	DA ₀₋₃	DB ₀₋₃
H	H	X	DA ₀₋₃	Q Register

L = LOW

H = HIGH

X = Don't Care

TABLE 2. ALU FUNCTIONS

I_4	I_3	I_2	I_1	Hex Code	ALU Functions
L	L	L	L	0	$I_0 = L$ Special Functions $I_0 = H$ $F_i = \text{HIGH}$
L	L	L	H	1	$F = S \text{ Minus } R \text{ Minus } 1 \text{ Plus } C_n$
L	L	H	L	2	$F = R \text{ Minus } S \text{ Minus } 1 \text{ Plus } C_n$
L	L	H	H	3	$F = R \text{ Plus } S \text{ Plus } C_n$
L	H	L	L	4	$F = S \text{ Plus } C_n$
L	H	L	H	5	$F = \overline{S} \text{ Plus } C_n$
L	H	H	L	6	$F = R \text{ Plus } C_n$
L	H	H	H	7	$F = \overline{R} \text{ Plus } C_n$
H	L	L	L	8	$F_i = \text{LOW}$
H	L	L	H	9	$F_i = \overline{R}_i \text{ AND } S_i$
H	L	H	L	A	$F_i = R_i \text{ EXCLUSIVE NOR } S_i$
H	L	H	H	B	$F_i = R_i \text{ EXCLUSIVE OR } S_i$
H	H	L	L	C	$F_i = R_i \text{ AND } S_i$
H	H	L	H	D	$F_i = R_i \text{ NOR } S_i$
H	H	H	L	E	$F_i = R_i \text{ NAND } S_i$
H	H	H	H	F	$F_i = R_i \text{ OR } S_i$

L = LOW

H = HIGH

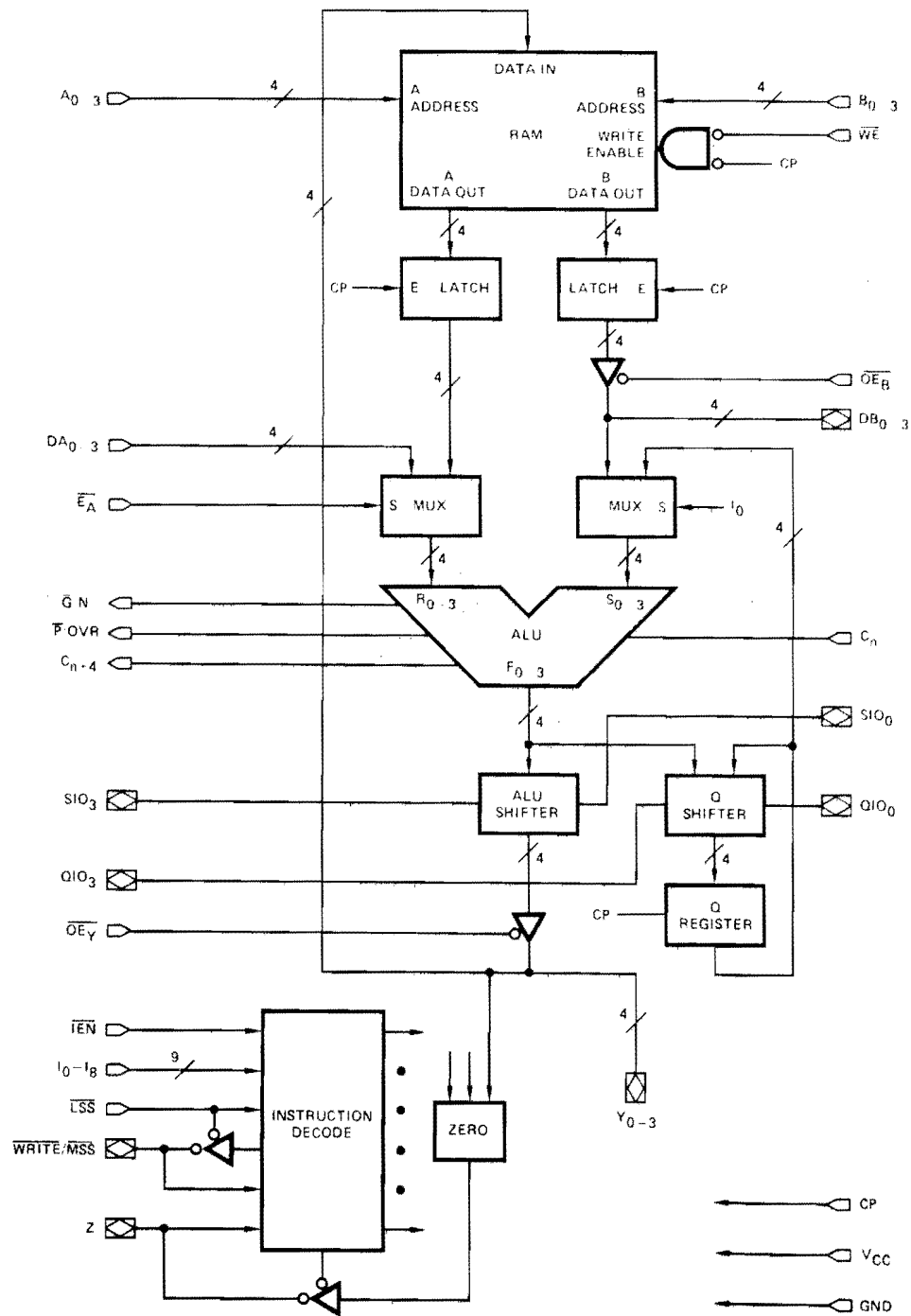
i = 0 to 3

generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multi-purpose $\overline{G}/N$ and $\overline{P}/OVR$ outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4} , $\overline{P}/OVR$, and $\overline{G}/N$ signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am2903 instruction.

ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure A). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

BLOCK DIAGRAM



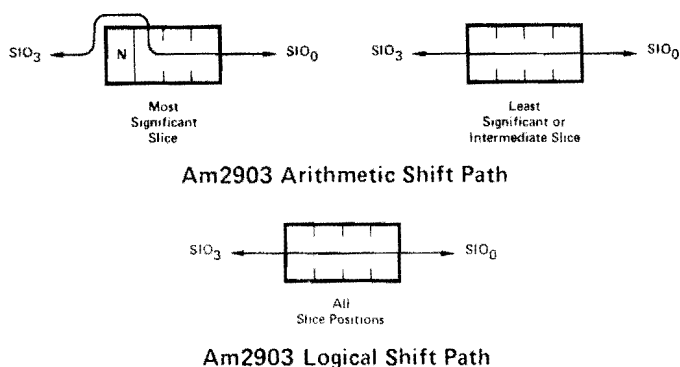


Figure A.

MPR-031

To some extent, the meaning of the SIO₀ and SIO₃ signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO₀ (sign) input can be extended through Y₀, Y₁, Y₂, Y₃ and propagated to the SIO₃ output.

A cascadable, five-bit parity generator/checker is designed into the Am2903 ALU shifter and provides ALU error detection capability. Parity for the F₀, F₁, F₂, F₃ ALU outputs and SIO₃ input is generated and, under instruction control, is made available at the SIO₀ output. Refer to the Am2903 applications section for a more detailed description of the Am2903 sign extension and parity generation/checking capability.

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am2903 executes instructions other than the nine special functions, the ALU shifter operation is determined by instruction bits I₈I₇I₆I₅. Table 3 defines the ALU shifter operation as a function of these four bits.

Q Register

The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some

applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO₀ and QIO₃ are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO₀ is a serial shift input and QIO₃ is a serial shift output. During a shift-down operation, QIO₃ is a serial shift input and QIO₀ is a serial shift output.

Double-length arithmetic and logical shifting capability is provided by the Am2903. The double-length shift is performed by connecting QIO₃ of the most significant slice to SIO₀ of the least significant slice, and executing an instruction which shifts both the ALU output and the Q Register.

The Q Register and shifter are controlled by the instruction inputs. Table 4 defines the Am2903 special functions and the operations which the Q Register and shifter perform for each. When the Am2903 executes instructions other than the nine special functions, the Q Register and shifter operation is controlled by instruction bits I₈I₇I₆I₅. Table 3 defines the Q Register and shifter operation as a function of these four bits.

Output Buffers

The DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the $\overline{OE_Y}$ input is LOW and are in the high-impedance state when $\overline{OE_Y}$ is HIGH. Likewise, the DB output buffers are enabled when the $\overline{OE_B}$ input is LOW and in the high-impedance state when $\overline{OE_B}$ is HIGH.

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y₀₋₃ pins are all LOW, whether they are driven from the Y output buffers or from an external source connected to the Y₀₋₃ pins. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am2903 instruction.

TABLE 3. ALU DESTINATION CONTROL FOR I₀ OR I₁ OR I₂ OR I₃ OR I₄ = HIGH, $\overline{IEN}$ = LOW.

				Hex Code	ALU Shifter Function	SIO ₃		Y ₃		Y ₂									
I ₈	I ₇	I ₆	I ₅			Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Y ₁	Y ₀	SIO ₀	Write	Q Reg & Shifter Function	QIO ₃	QIO ₀	
L	L	L	L	0	Arith F2→Y	Input	Input	F ₃	SIO ₃	SIO ₃	F ₃	F ₂	F ₁	F ₀	L	Hold	Hi-Z	Hi-Z	
L	L	L	H	1	Log F2→Y	Input	Input	SIO ₃	SIO ₃	F ₃	F ₃	F ₂	F ₁	F ₀	L	Hold	Hi-Z	Hi-Z	
L	L	H	L	2	Arith F2→Y	Input	Input	F ₃	SIO ₃	SIO ₃	F ₃	F ₂	F ₁	F ₀	L	Log Q2→Q	Input	Q ₀	
L	L	H	H	3	Log F2→Y	Input	Input	SIO ₃	SIO ₃	F ₃	F ₃	F ₂	F ₁	F ₀	L	Log Q2→Q	Input	Q ₀	
L	H	L	L	4	F→Y	Input	Input	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Parity	L	Hold	Hi-Z	Hi-Z	
L	H	L	H	5	F→Y	Input	Input	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Parity	H	Log Q2→Q	Input	Q ₀	
L	H	H	L	6	F→Y	Input	Input	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Parity	H	F→Q	Hi-Z	Hi-Z	
L	H	H	H	7	F→Y	Input	Input	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Parity	L	F→Q	Hi-Z	Hi-Z	
H	L	L	L	8	Arith 2F→Y	F ₂	F ₃	F ₃	F ₂	F ₁	F ₁	F ₀	SIO ₀	Input	L	Hold	Hi-Z	Hi-Z	
H	L	L	H	9	Log 2F→Y	F ₃	F ₃	F ₂	F ₂	F ₁	F ₁	F ₀	SIO ₀	Input	L	Hold	Hi-Z	Hi-Z	
H	L	H	L	A	Arith 2F→Y	F ₂	F ₃	F ₃	F ₂	F ₁	F ₁	F ₀	SIO ₀	Input	L	Log 2Q→Q	Q ₃	Input	
H	L	H	H	B	Log 2F→Y	F ₃	F ₃	F ₂	F ₂	F ₁	F ₁	F ₀	SIO ₀	Input	L	Log 2Q→Q	Q ₃	Input	
H	H	L	L	C	F→Y	F ₃	F ₃	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Hi-Z	H	Hold	Hi-Z	Hi-Z	
H	H	L	H	D	F→Y	F ₃	F ₃	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Hi-Z	H	Log 2Q→Q	Q ₃	Input	
H	H	H	L	E	SIO ₀ →Y ₀ , Y ₁ , Y ₂ , Y ₃	SIO ₀	SIO ₀	SIO ₀	SIO ₀	SIO ₀	SIO ₀	SIO ₀	SIO ₀	Input	L	Hold	Hi-Z	Hi-Z	
H	H	H	H	F	F→Y	F ₃	F ₃	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Hi-Z	L	Hold	Hi-Z	Hi-Z	

Parity = $F_3 \nabla F_2 \nabla F_1 \nabla F_0 \nabla SIO_3$
 ∇ = Exclusive OR

L = LOW
H = HIGH

Hi-Z = High Impedance

TABLE 4. SPECIAL FUNCTIONS: $I_0 = I_1 = I_2 = I_3 = I_4 = \text{LOW}$, $\overline{\text{IEN}} = \text{LOW}$

I_8	I_7	I_6	I_5	Hex Code	Special Function	ALU Function	ALU Shifter Function	SIO ₃		SIO ₀	Q Reg & Shifter Function	QIO ₃	QIO ₀	WRITE
								Most Sig. Slice	Other Slices					
L	L	L	L	0	Unsigned Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log. $F/2 \rightarrow Y$ (Note 1)	Hi-Z	Input	F_0	Log. $Q/2 \rightarrow Q$	Input	Q_0	L
L	L	H	L	2	Two's Complement Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log. $F/2 \rightarrow Y$ (Note 2)	Hi-Z	Input	F_0	Log. $Q/2 \rightarrow Q$	Input	Q_0	L
L	H	L	L	4	Increment by One or Two	$F = S + 1 + C_n$	$F \rightarrow Y$	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L	H	L	H	5	Sign/Magnitude Two's Complement	$F = S + C_n$ if $Z = L$ $F = \overline{S} + C_n$ if $Z = H$	$F \rightarrow Y$ (Note 3)	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L	H	H	L	6	Two's Complement Multiply, Last Cycle	$F = S + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log. $F/2 \rightarrow Y$ (Note 2)	Hi-Z	Input	F_0	Log. $Q/2 \rightarrow Q$	Input	Q_0	L
H	L	L	L	8	Single Length Normalize	$F = S + C_n$	$F \rightarrow Y$	F_3	F_3	Hi-Z	Log. $2Q \rightarrow Q$	Q_3	Input	L
H	L	H	L	A	Double Length Normalize and First Divide Op.	$F = S + C_n$	Log $2F \rightarrow Y$	$R_3 \vee F_3$	F_3	Input	Log. $2Q \rightarrow Q$	Q_3	Input	L
H	H	L	L	C	Two's Complement Divide	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log. $2F \rightarrow Y$	$\overline{R_3} \vee \overline{F_3}$	F_3	Input	Log. $2Q \rightarrow Q$	Q_3	Input	L
H	H	H	L	E	Two's Complement Divide, Correction and Remainder	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	$F \rightarrow Y$	F_3	F_3	Hi-Z	Log. $2Q \rightarrow Q$	Q_3	Input	L

NOTES: 1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
 2. At the most significant slice only, $F_3 \vee \text{OVR}$ is internally gated to the Y_3 output.
 3. At the most significant slice only, $S_3 \vee F_3$ is generated at the Y_3 output.
 4. Op codes 1, 3, 7, 9, B, D, and F are reserved for future use.

L = LOW
 H = HIGH
 X = Don't Care

Hi-Z = High Impedance
 $\vee$ = Exclusive OR
 Parity = $\text{SIO}_3 \vee F_3 \vee F_2 \vee F_1 \vee F_0$

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine Instruction inputs, I_0 – I_8 ; the Instruction Enable input, $\overline{\text{IEN}}$; the $\overline{\text{LSS}}$ input; and the $\overline{\text{WRITE/MSS}}$ input/output.

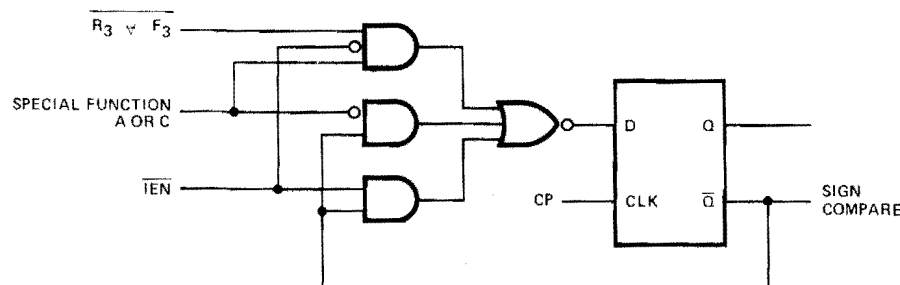
The $\overline{\text{WRITE}}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{\text{WRITE}}$ output as a function of the Am2903 instruction inputs.

When $\overline{\text{IEN}}$ is HIGH, the $\overline{\text{WRITE}}$ output is forced HIGH and the Q Register and Sign Compare Flip-Flop contents are preserved.

When $\overline{\text{IEN}}$ is LOW, the $\overline{\text{WRITE}}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the Am2903 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am2903 divide operation (see Figure B).

Programming the Am2903 Slice Position

Tying the $\overline{\text{LSS}}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{\text{WRITE}}$ output signal onto the $\overline{\text{WRITE/MSS}}$ bidirectional I/O pin. When $\overline{\text{LSS}}$ is tied HIGH, the $\overline{\text{WRITE/MSS}}$ pin becomes an input pin; tying the $\overline{\text{WRITE/MSS}}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS).



The sign compare signal appears at the Z output of the most significant slice during special functions C, D and E, F. Refer to Table 5.

Figure B. Sign Compare Flip-Flop.

TABLE 5. Am2903 STATUS OUTPUTS

(Hex) 18 ¹ 7 ¹ 6 ¹ 5	(Hex) 14 ¹ 3 ¹ 2 ¹ 1 ¹	I ₀	G _i (i=0 to 3)	P _i (i=0 to 3)	C _{n+4}	P/OVR		G/N		Z		
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Intermediate Slice	Least Sig. Slice
X	0	H	0	1	0	0	0	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	1	X	$\bar{R}_i \wedge S_i$	$\bar{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	2	X	$R_i \wedge \bar{S}_i$	$R_i \vee \bar{S}_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	3	X	$R_i \wedge S_i$	$\bar{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	4	X	0	$\bar{S}_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	5	X	0	$\bar{S}_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	6	X	0	$\bar{R}_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	7	X	0	$\bar{R}_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	8	X	0	1	0	0	0	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	9	X	$\bar{R}_i \wedge S_i$	1	0	0	0	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	B	X	$\bar{R}_i \wedge \bar{S}_i$	$\bar{R}_i \vee \bar{S}_i$	0	0	0	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	D	X	$\bar{R}_i \wedge \bar{S}_i$	1	0	0	0	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	F	X	$\bar{R}_i \wedge \bar{S}_i$	1	0	0	0	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
0	0	L	0 if Z=L $\bar{R}_i \wedge S_i$ if Z=H	S_i if Z=L $\bar{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	Input	Input	Q ₀
2	0	L	0 if Z=L $\bar{R}_i \wedge S_i$ if Z=H	S_i if Z=L $\bar{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	Input	Input	Q ₀
4	0	L	See Note 1	See Note 2	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
5	0	L	0	S_i if Z=L $\bar{S}_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F_3 if Z=L $F_3 \nabla S_3$ if Z=H	$\bar{G}$	S ₃	Input	Input
6	0	L	0 if Z=L $\bar{R}_i \wedge S_i$ if Z=H	S_i if Z=L $\bar{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	Input	Input	Q ₀
8	0	L	0	S_i	See Note 3	Q ₂ ∇ Q ₁	$\bar{P}$	Q ₃	$\bar{G}$	Q ₀ Q ₁ Q ₂ Q ₃	Q ₀ Q ₁ Q ₂ Q ₃	Q ₀ Q ₁ Q ₂ Q ₃
A	0	L	0	S_i	See Note 4	F ₂ ∇ F ₁	$\bar{P}$	F ₃	$\bar{G}$	See Note 5	See Note 5	See Note 5
C	0	L	$R_i \wedge S_i$ if Z=L $\bar{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\bar{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	Sign Compare FF Output	Input	Input
E	0	L	$R_i \wedge S_i$ if Z=L $\bar{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\bar{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\bar{P}$	F ₃	$\bar{G}$	Sign Compare FF Output	Input	Input

L = LOW = 0

H = HIGH = 1

V = OR

 $\wedge$ = AND ∇ = EXCLUSIVE ORP = P₃P₂P₁P₀G = G₃G₂G₁G₀P₃P₂P₁P₀C_{n+3} = G₂G₁P₂VG₀P₁P₂VC_nP₀P₁P₂NOTES: 1. If LSS is LOW, G₀ = S₀ and G_{1,2,3} = 0If LSS is HIGH, G_{0,1,2,3} = 02. If LSS is LOW, P₀ = 1 and P_{1,2,3} = S_{1,2,3}If LSS is HIGH, P_i = S_i3. At the most significant slice, C_{n+4} = Q₃ ∇ Q₂At other slices, C_{n+4} = G $\vee$ PC_n4. At the most significant slice, C_{n+4} = F₃ ∇ F₂At other slices, C_{n+4} = G $\vee$ PC_n5. Z = Q₀Q₁Q₂Q₃F₀F₁F₂F₃**Am2903 SPECIAL FUNCTIONS**

The Am2903 provides nine Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am2903. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

Refer to Am2903 applications section for a more detailed description of these Special Functions.

PIN DEFINITIONS

A₀₋₃ Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.

B₀₋₃ Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.

$\overline{WE}$ The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.

DA₀₋₃ A four-bit external data input which can be selected as one of the Am2903 ALU operand sources; DA₀ is the least significant bit.

$\overline{EA}$ A control input which, when HIGH, selects DA₀₋₃ and, when LOW, selects RAM output A as the ALU R operand.

DB₀₋₃ A four-bit external data input/output. Under control of the $\overline{OE_B}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.

$\overline{OE_B}$ A control input which, when LOW, enables RAM output B onto the DB₀₋₃ lines and, when HIGH, disables the RAM output B tri-state buffers.

C_n The carry-in input to the Am2903 ALU.

I₀₋₈ The nine instruction inputs used to select the Am2903 operation to be performed.

$\overline{IEN}$ The instruction enable input which, when LOW, enables the $\overline{WRITE}$ output and allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q Register and Sign Compare flip-flop are in the hold mode.

C_{n+4} This output generally indicates the carry-out of the Am2903 ALU. Refer to Table 5 for an exact definition of this pin.

$\overline{G/N}$ A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.

$\overline{P/OVR}$ A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.

Z An open-collector input/output pin which, when HIGH, generally indicates the Y₀₋₃ outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.

SIO₀, SIO₃ Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO₀ is an input and SIO₃ an output. During a shift-down operation, SIO₃ is an input and SIO₀ is an output. Refer to Tables 3 and 4 for an exact definition of these pins.

QIO₀, QIO₃ Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO₀ and SIO₃. Refer to Tables 3 and 4 for an exact definition of these pins.

$\overline{LSS}$ An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am2903 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE/MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.

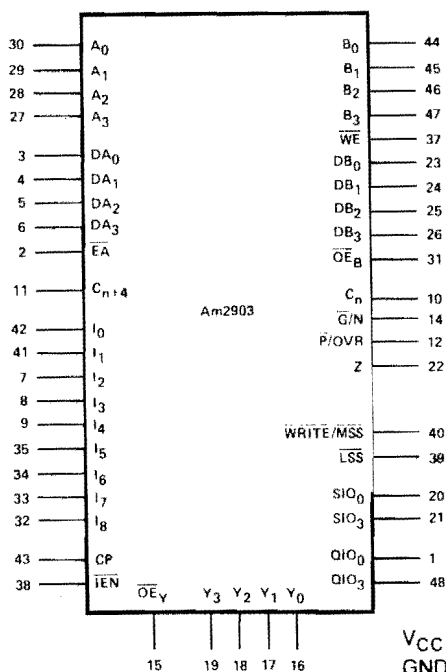
$\overline{WRITE/MSS}$ When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE/MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).

Y₀₋₃ Four data inputs/outputs of the Am2903. Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.

$\overline{OE_Y}$ A control input which, when LOW, enables the ALU shifter output data onto the Y₀₋₃ lines and, when HIGH, disables the Y₀₋₃ three-state output buffers.

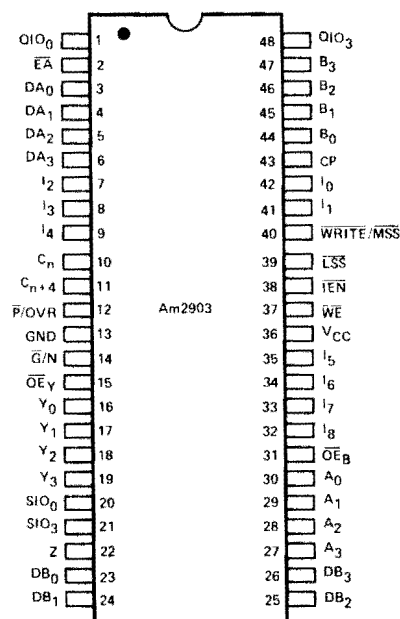
CP The clock input to the Am2903. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

LOGIC SYMBOL



CONNECTION DIAGRAM

Top View

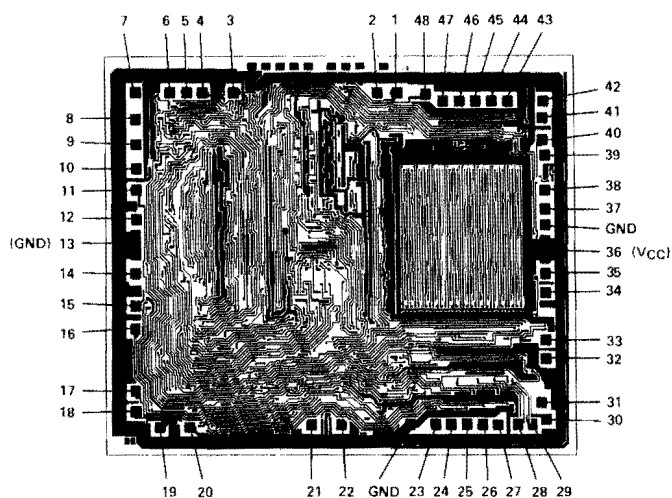


Note: Pin 1 is marked for orientation.

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MPR-034

Metallization and Pad Layout



DIE SIZE 0.163" X 0.197"

Note: Pin numbers correspond to DIP package.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2903DC	D-48	C	C-1
AM2903DC-B	D-48	C	B-1
AM2903DM	D-48	M	C-3
AM2903DM-B	D-48	M	B-3
AM2903FM	F-48	M	C-3
AM2903FM-B	F-48	M	B-3

- Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = -55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2903 OPERATING RANGE

P/N	Range	Temperature	V _{CC}
Am2903PC, DC	COM'L	T _A = 0°C to +70°C	V _{CC} = 5.0V ±5% (MIN. = 4.75V, MAX. = 5.25V)
Am2903DM, FM	MIL	T _C = -55°C to +125°C	V _{CC} = 5.0V ±10% (MIN. = 4.50V, MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN. V _{IN} = V _{IH} or V _{IL} I _{OH} = -1.6mA Y ₀ -Y ₃ , $\bar{G}/N$ I _{OH} = -800μA DB ₀₋₃ , $\bar{P}/OVR$ SIO ₀ , SIO ₃ , QIO ₀ , QIO ₃ , WRITE, C _{n+4}	2.4			Volts
I _{CEX}	Output Leakage Current for Z Output (Note 4)	V _{CC} = MIN., V _{OH} = 5.5V V _{IN} = V _{IH} or V _{IL}			250	μA
V _{OL}	Output LOW Voltage	V _{CC} = MIN. V _{IN} = V _{IH} or V _{IL} Y ₀ , Y ₁ , Y ₂ Y ₃ , Z DB ₀ , DB ₁ , DB ₂ , DB ₃ $\bar{G}/N$ $\bar{P}/OVR$ C _{n+4} , SIO ₀ SIO ₃ , QIO ₀ QIO ₃ , WRITE I _{OL} = 20mA (COM'L) I _{OL} = 16mA (MIL) I _{OL} = 12mA (COM'L) I _{OL} = 8.0mA (MIL) I _{OL} = 18mA I _{OL} = 10mA I _{OL} = 8.0mA			0.5 0.5 0.5 0.5	Volts
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)	2.0			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)			0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = MIN., I _{IN} = -18mA			-1.5	Volts
I _{IL}	Input LOW Current	V _{CC} = MAX., V _{IN} = 0.5V (Note 4) C _n Y ₀ , Y ₁ , Y ₂ , Y ₃ I ₀ , I ₁ , I ₂ , I ₃ , I ₄ , DA ₀ , DA ₁ , DA ₂ , DA ₃ , SIO ₀ SIO ₃ , QIO ₀ , QIO ₃ , MSS, DB ₀ , DB ₁ , DB ₂ , DB ₃ All other inputs			2.50 1.08 0.72 0.36	mA
I _{IH}	Input HIGH Current	V _{CC} = MAX., V _{IN} = 2.7V (Note 4) C _n Y ₀ , Y ₁ , Y ₂ , Y ₃ I ₀ -I ₄ , DA ₀ -DA ₃ SIO ₀ , SIO ₃ , QIO ₀ , QIO ₃ , DB ₀₋₃ , MSS All other inputs			120 110 40 90 20	μA
I _I	Input HIGH Current	V _{CC} = MAX., V _{IN} = 5.5V			1.0	mA
I _{OZH} I _{OZL}	Off State (HIGH Impedance) Output Current	V _{CC} = MAX., (Note 4) Y ₀ -Y ₃ DB ₀₋₃ , QIO ₀ , QIO ₃ , SIO ₀ , SIO ₃ , MSS/IS	V _O = 2.4V V _O = 0.5V V _O = 2.4V V _O = 0.5V		110 -1130 90 -770	μA
I _{OS}	Output Short Circuit Current (Note 3)	V _{CC} = MAX + 0.5V V _O = 0.5V	-30		-85	mA
I _{CC}	Power Supply Current (Note 5)	V _{CC} = MAX. T _A = 25°C COM'L MIL T _A = 0 to 70°C T _A = 70°C T _C = -55 to 125°C T _C = 125°C		220	335 350 291 395 258	mA

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y₀₋₃, DB₀₋₃, SIO_{0,3}, QIO_{0,3} and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

SWITCHING CHARACTERISTICS (Typical Room Temperature Performance)

Tables I, II, and III define the nominal timing characteristics of the Am2903 at 25°C and 5.0V. The Tables divide the parameters into three types: pulse characteristics for the clock and write enable, combinational delays from input to output, and set-up and hold times relative to the clock and write pulse.

Measurements are made at 1.5V with $V_{IL} = 0V$ and $V_{IH} = 3.0V$. For three-state disable tests, $C_L = 5.0pF$ and measurement is to 0.5V change on output voltage level.

TABLE I
Write Pulse and Clock Characteristics

Time	
Minimum Time CP and $\overline{WE}$ both LOW to write	30ns
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	50ns

TABLE II
Combinational Propagation Delays, All in ns.
Outputs Fully Loaded. $C_L = 50pf$ (except output disable tests)

To Output From Input	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	QIO_0, QIO_3	SIO_0	SIO_3	SIO_3 (Parity)
A, B Addresses (Arith. Mode)	65	60	55	75	64	70	33	—	—	61	69	87
A, B Addresses (Logic Mode)	56	—	46	67	56	—	33	—	—	55	64	81
DA, DB Inputs (Logic Mode)	39	—	25	48	38	—	—	—	—	36	47	56
DA, DB Inputs (Arith. Mode)	39	37	26	52	38	51	—	—	—	36	47	60
$\overline{EA}$	44	38	29	54	44	53	—	—	—	42	52	—
C_n	25	21	—	39	20	38	—	—	—	21	25	48
I_0	39	35	24	48	37	48	—	*15	—	41	46	—
I_{4321}	45	43	32	55	44	55	—	*17	—	45	51	—
I_{8765}	25	—	—	37	—	—	—	18	22	24	27	—
$\overline{I}_{EN}$	—	—	—	—	—	—	—	10	—	—	—	—
$\overline{OEB}$ Enable/Disable	—	—	—	—	—	—	7	—	—	—	—	—
$\overline{OEY}$ Enable/Disable	10	—	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	13	—	—	—	—	—	—	—	—	—	12	18
Clock	58	52	40	72	56	72	24	—	28	55	63	76

*Applies only when leaving special functions.

TABLE III
Set-Up and Hold Times (All in ns)
CAUTION: READ NOTES TO TABLE III.
NA = Not Applicable; no timing constraint.

Input	With Respect to to this Signal	HIGH-to-LOW		LOW-to-HIGH		Comment
		Set-up	Hold	Set-up	Hold	
Y	Clock	NA	NA	10	0	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	5	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	30	0	To Write into RAM
A,B as Sources	Clock	20	0	NA	NA	See Note 3
B as a Destination	Clock and $\overline{WE}$ both LOW	0	Note 4	Note 4	0	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	10	0	To Shift Q
I_{8765}	Clock	30	Note 5	Note 5	0	
$\overline{I}_{EN}$ HIGH	Clock	10	Note 2	Note 2	0	To Prevent Writing
$\overline{I}_{EN}$ LOW	Clock	NA	NA	10	0	To Write into Q

Notes To Table III. (Set-up and Hold Times)

1. For set-up times from all inputs not specified in Table III, the set-up time is computed by calculating the delay to stable Y outputs and then allowing the Y set-up time. Even if the RAM is not being loaded, the Y set-up time is necessary to set-up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock

has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.

3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.

USING THE Am2903

Am2903 APPLICATIONS

The Am2903 is designed to be used in microprogrammed systems. Figure 1 illustrates a recommended architecture. The control and data inputs to the Am2903 normally will all come from registers clocked at the same time as the Am2903. The register inputs come from a ROM or PROM — the "microprogram store". This memory contains sequences of microinstructions which apply the proper control signals to the Am2903's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2910 Microprogram Sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2910 is controlled by some of the bits coming from the microprogram store. Essentially, these bits are the "next instruction" control.

One Level Pipeline Based System

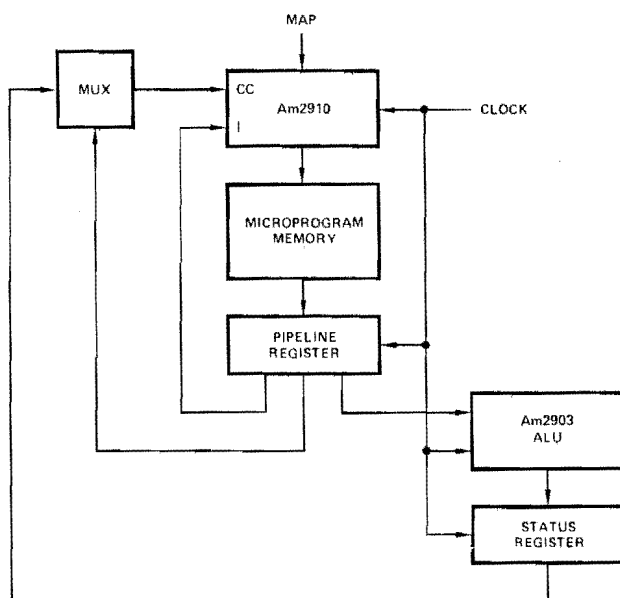


Figure 1. Typical Microprogram Architecture.

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Note that with the microprogram register in between the microprogram memory store and the Am2903's, a microinstruction accessed on one cycle is executed on the next cycle. As one microinstruction is executed, the next microinstruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2903's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

Expansion of the Am2903

The Am2903 is a four-bit CPU slice. Any number of Am2903's can be interconnected to form CPU's of 8, 16, 32, or more bits, in four-bit increments. Figure 2 illustrates the interconnection of four Am2903's to form a 16-bit CPU, using ripple carry.

With the exception of the carry interconnection, all expansion schemes are the same. The QIO_3 and SIO_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the QIO_0 and SIO_0 pins of the adjacent more significant device. These connections allow the Q Registers of all Am2903's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to a shift multiplexer which can be controlled by the microcode to select the appropriate input signals to the shift inputs.

Device 1 has been defined as the least significant slice (LSS) and its $\overline{LSS}$ pin has accordingly been grounded. The Write/Most Significant Slice ($\overline{WRITE/MSS}$) pin of device 1 is now defined as being the Write output, which may now be used to drive the write enable ($\overline{WE}$) signal common to the four devices. Devices 2 and 3 are designated as intermediate slices and hence the $\overline{LSS}$ and $\overline{WRITE/MSS}$ pins are tied HIGH. Device 4 is designated the most significant slice ($\overline{MSS}$) with the $\overline{LSS}$ pin tied HIGH and the $\overline{WRITE/MSS}$ pin held LOW. The open collector, bidirectional Z pins are tied together for detecting zero or for inter-chip communication for some special instruction. The Carry-Out (C_{n+4}) is connected to the Carry-In (C_n) of the next chip in the case of ripple carry. For a faster carry scheme, an Am2902 may be employed (as shown in Figure 3) such that the $\overline{G}$ and $\overline{P}$ outputs of the Am2903 are connected to the appropriate $\overline{G}$ and $\overline{P}$ inputs of the Am2902, while the C_{n+x} , C_{n+y} , and C_{n+z} outputs of the Am2902 are connected to the C_n input of the appropriate Am2903. Note that $\overline{G}/N$ and $\overline{P}/OVR$ pin functions are device dependent. The most significant slice outputs N and OVR while all other slices output $\overline{G}$ and $\overline{P}$.

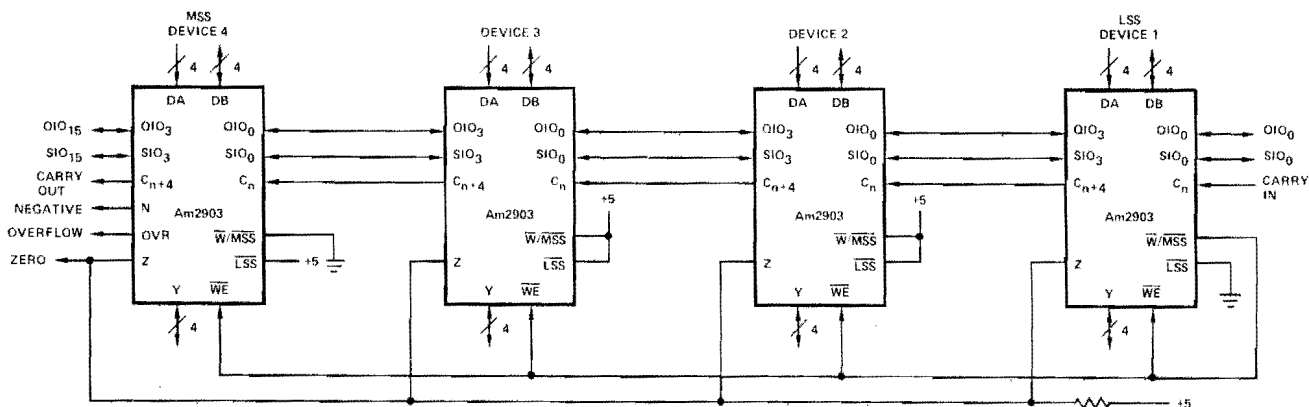


Figure 2. 16-Bit CPU with Ripple Carry.

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The $\overline{\text{IEN}}$ pin of the Am2903 allows the option of conditional instruction execution. If $\overline{\text{IEN}}$ is LOW, all internal clocking is enabled, allowing the latches, RAM, and Q Register to function. If $\overline{\text{IEN}}$ is HIGH, the RAM and Q Register are disabled. The RAM is controlled by $\overline{\text{IEN}}$ if $\overline{\text{WE}}$ is connected to the $\overline{\text{WRITE}}$ output.

It would be appropriate at this point to mention that the Am2903 may be microcoded to work in either two-or three-address architecture modes. The two-address modes allow $A+B \rightarrow B$ while the three-address mode makes possible $A+B \rightarrow C$. Implementation of a three-address architecture is made possible by varying the timing of $\overline{\text{IEN}}$ in relationship to the external clock and changing the B address as shown in Figure 4. This technique is discussed in more detail under Memory Expansion.

Parity

The Am2903 computes parity on a chosen word when the instruction bits I_{5-8} have the values of 4_{16} to 7_{16} as shown in Table 3. The computed parity is the result of the exclusive OR of the individual ALU outputs and SIO_3 . Parity output is found on SIO_0 . Parity between devices may be cascaded by the interconnection of the SIO_0 and SIO_3 ports of the devices as shown in Figure 3. The equation for the parity output at SIO_0 port of device 1 is given by $\text{SIO}_0 = F_{15} \vee F_{14} \vee F_{13} \vee \dots \vee F_1 \vee F_0 \vee \text{SIO}_{15}$.

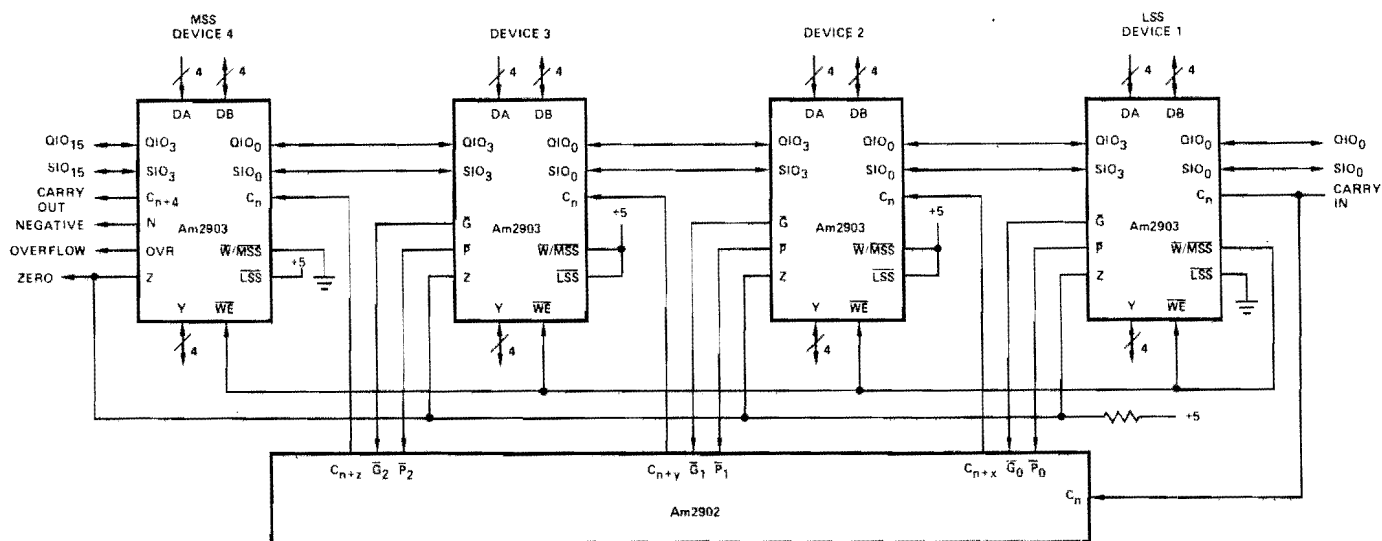


Figure 3. 16-Bit CPU with Carry Look Ahead.

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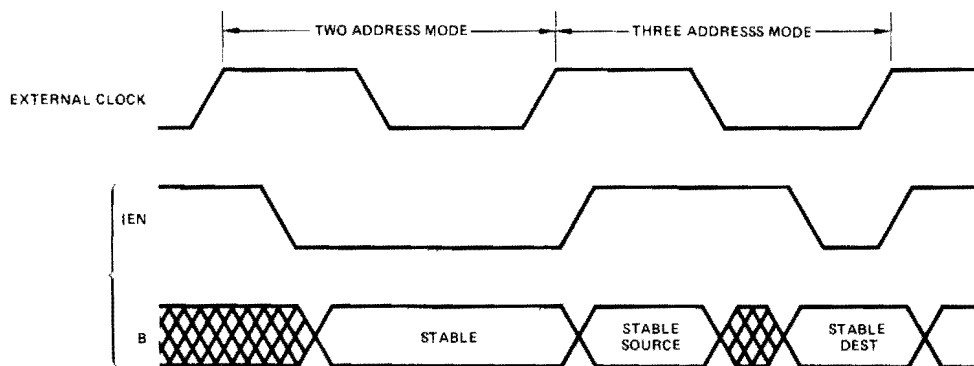


Figure 4. Relationship of $\overline{\text{IEN}}$ and Clock During Two Address and Three Address Modes.

MPR-038

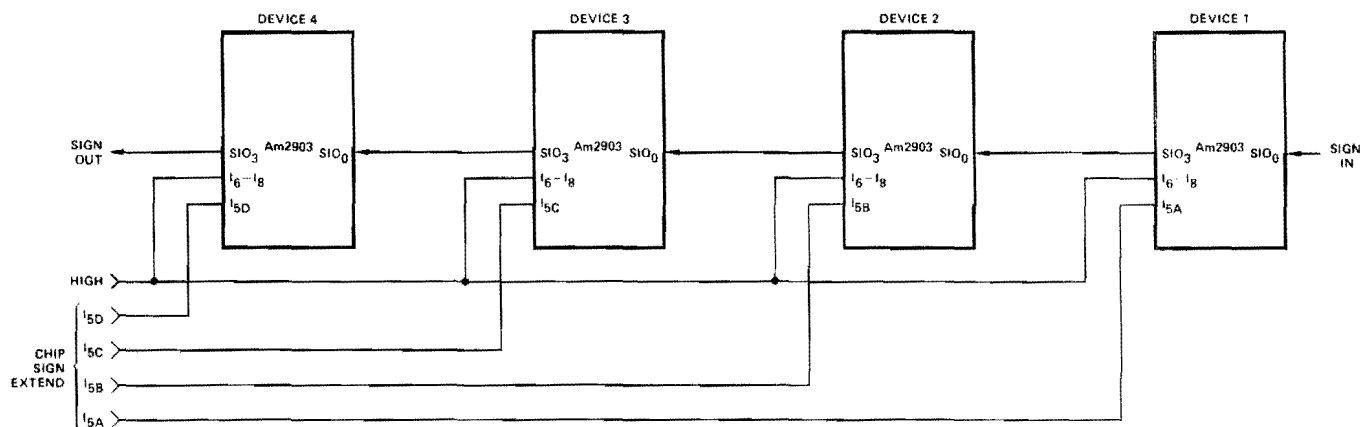


Figure 5. Sign Extend.

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Sign Extend

Sign extension across any number of Am2903 devices can be done in one microcycle. Referring again to the table of instructions (Table 3), the sign extend instruction (Hex instruction E) on I_{5-8} causes the sign present at the SIO_0 port of a device to be extended across the device and appear at the SIO_3 port and at the Y outputs. If the least significant bit of the instruction (bit I_5) is HIGH, Hex instruction F is present on I_{5-8} , commanding a shifter pass instruction. At this time, F_3 of the ALU is present on the SIO_3 output pin. It is then possible to control the extension of the sign across chip boundaries by controlling the state of I_5 when I_{6-8} are HIGH. Figure 5 outlines the Am2903 in sign extend mode. With I_{6-8} held HIGH, the individual chip sign extend is controlled by I_{5A-D} . If, for example, I_{5A} and I_{5B} are HIGH while I_{5C} and I_{5D} are LOW, the signal present at the boundaries of devices 2 and 3 (F_3 of device 2) will be extended across devices 3 and 4 at the SIO_3 pin of device 4. The output of the four devices will be available at their respective Y data ports. The next positive edge of the clock will load the Y outputs into the address selected by the B port. Hence, the results of the sign extension is stored in the RAM.

SPECIAL FUNCTIONS

When $I_{0-4} = 0$, the Am2903 is in the Special Function mode. In this mode, both the source and destination are controlled by I_{5-8} . The Special Functions are in essence special microinstructions that are used to reduce the number of microcycles needed to execute certain functions in the Am2903.

Normalization, Single- and Double-Length

Normalization is used as a means of referencing a number to a fixed radix point. Normalization strips out all leading sign bits such that the two bits immediately adjacent to the radix point are of opposite polarity.

Normalization is commonly used in such operations as fixed-to-floating point conversion and division. The Am2903 provides for normalization by using the Single-Length and Double-Length Normalize commands. Figure 6a represents the Q Register of a 16-bit processor which contains a positive number. When the Single-Length Normalize command is applied, each positive edge of the clock will cause the bits to shift toward the most significant bit (bit 15) of the Q Register. Zeros are shifted in via the QIO_0 port. When the bits on either side of the radix point (bits 14 and 15) are of opposite value, the number is considered to be normalized as shown in Figure 6b. The event of normalization is externally indicated by a HIGH level on the C_{n+4} pin of the most significant slice ($C_{n+4} \text{ MSS} = Q_3 \text{ MSS} \nabla Q_2 \text{ MSS}$).

RADIX															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Q REGISTER															
0	0	0	0	1	1	1	1	1	0	0	1	0	0	1	1
MSS												LSS			
DEVICE 4				DEVICE 3				DEVICE 2				DEVICE 1			

a) Unnormalized Positive Number.

RADIX															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Q REGISTER															
0	1	1	1	1	1	0	0	1	0	0	1	1	0	0	0
MSS												LSS			

b) Normalized Positive Number.

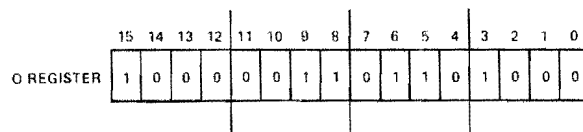
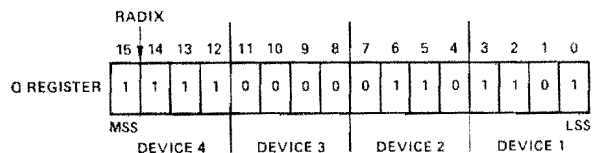
Figure 6.

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There are also provisions made for a normalization indication via the OVR pin one microcycle before the same indication is available on the C_{n+4} pin ($\text{OVR} = Q_2 \text{ MSS} \nabla Q_1 \text{ MSS}$). This is for use in applications that require a stage of register buffering of the normalization indication.

Since a number comprised of all zeros is not considered for normalization, the Am2903 indicates when such a condition arises. If the Q Register is zero and the Single-Length Normalization command is given, a HIGH level will be present on the Z line. The sign output, N, indicates the sign of the number stored in the Q register, $Q_3 \text{ MSS}$. An unnormalized negative number (Figure 7a) is normalized in the same manner as a positive number. The results of single-length normalization are shown in Figure 7b. The device interconnection for single-length normalization is outlined in Figure 8. During single length normalization, the number of shifts performed to achieve normalization can be counted and stored in one of the working registers. This can be achieved by forcing a HIGH at the C_n input of the least significant slice, since during this special function the ALU performs the function $[B] + C_n$ and the result is stored in B.

Normalizing a double-length word can be done with the Double-Length Normalize command which assumes that a user-selected RAM Register contains the most significant portion of the word to be normalized while the Q Register holds the least significant half (Figure 9). The device interconnection for double-length normalization is shown in Figure 10. The C_{n+4} , OVR, N, and Z outputs of the most significant slice perform the same functions in double-length normalization as they did in single-length normalization except that C_{n+4} , OVR, and N are derived from the output of the ALU of the most significant slice in the case of double-length normalization, instead of the Q Register of the most significant



a) Unnormalized Negative Single Length Number.

b) Normalized Negative Single Length Number.

Figure 7.

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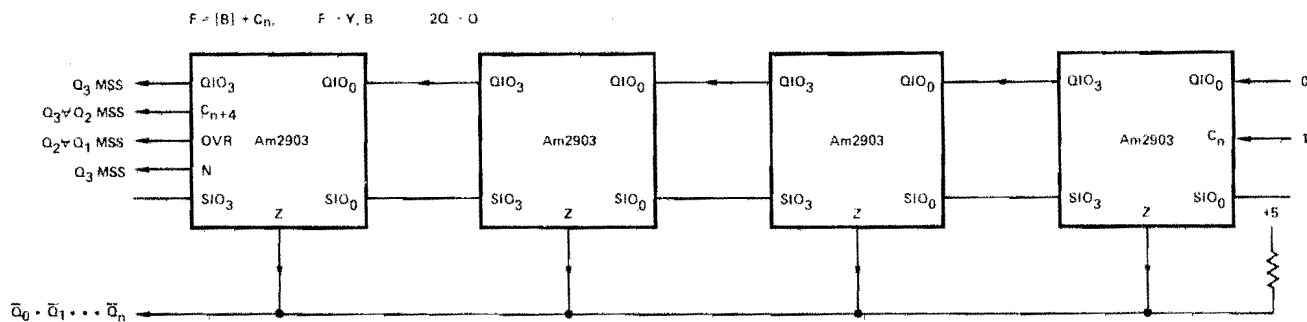


Figure 8. Single Length Normalize.

MPR-042

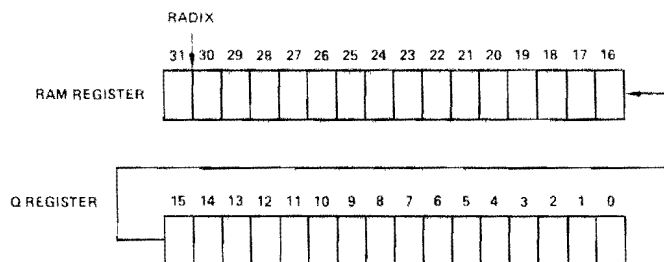


Figure 9. Double Length Word.

MPR-043

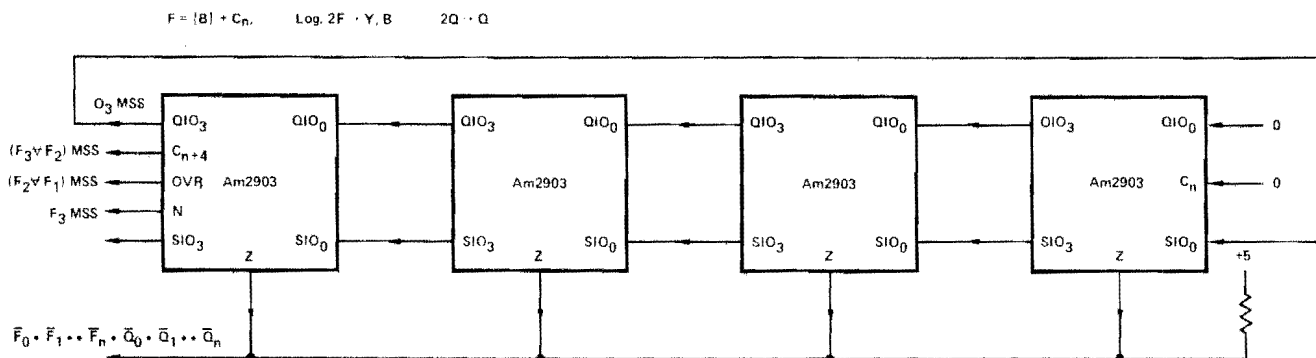


Figure 10. Double Length Normalize.

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slice as in single-length normalization. A high-level Z line in double-length normalization reveals that the outputs of the ALU and Q Register are both zero, hence indicating that the double-length word is zero.

When double-length normalization is being performed, shift counting is done either with an extra microcycle or with an external counter.

Sign Magnitude, Two's Complement Conversion

As part of the special instruction set, the Am2903 can convert between two's complement and sign/magnitude representations. Figure 11 illustrates the interconnection needed for sign magnitude/two's complement conversion. The word to be converted is applied to the S input port of the ALU (from the RAM B port or the DB I/O port). The C_n input of device 1 is connected to the Z pin. The sign bit (S_3 MSS) is brought out on the Z line and informs the other ALU's if the conversion is being performed on a negative or positive number. If the number to be converted is the most negative number in two's complement [i.e., $100 \dots 00 (-2^n)$], an overflow indication will occur. This is because -2^n is one greater than any number that can be represented in sign magnitude notation and hence an attempted conversion to sign magnitude from -2^n will cause an overflow. When minus zero in sign magnitude notation ($100 \dots 0$) is converted to two's complement notation, the correct result is obtained ($0 \dots 0$).

Increment by One or Two

Incrementation by One or Two is made possible by the Special Function of the same name. This command is quite useful in the case of byte addressable words. Referencing Figure 12, a word may be incremented by one if C_n is LOW or incremented by two if C_n is HIGH.

Unsigned Multiply

This Special Function allows for easy implementation of unsigned multiplication. Figure 13 is the unsigned multiply flow chart. The algorithm requires that initially the RAM word addressed by Address port B be zero, that the multiplier be in the Q Register, and that the multiplicand be in the register addressed by Address port A. The initial conditions for the execution of the algorithm are that: 1) register R_0 be reset to zero; 2) the multiplicand be in R_1 ; and 3) the multiplier be in R_2 . The first operation transfers the multiplier, R_2 , to the Q Register. The Unsigned Multiply instruction is then executed 16 times. During the Unsigned Multiply instruction, R_0 is addressed by RAM address port B and the multiplicand is addressed by RAM address port A.

When the unsigned Multiply command is given, the Z pin of device 1 becomes an output while the Z pins of the remaining devices are specified as inputs as shown in Figure 15. The Z output of device 1 is the same state as the least significant bit of the multiplier in the Q Register. The Z output of device 1 informs the ALU's of all the slices, via their Z pins, to add the partial product (referenced by the B address port) to the mul-

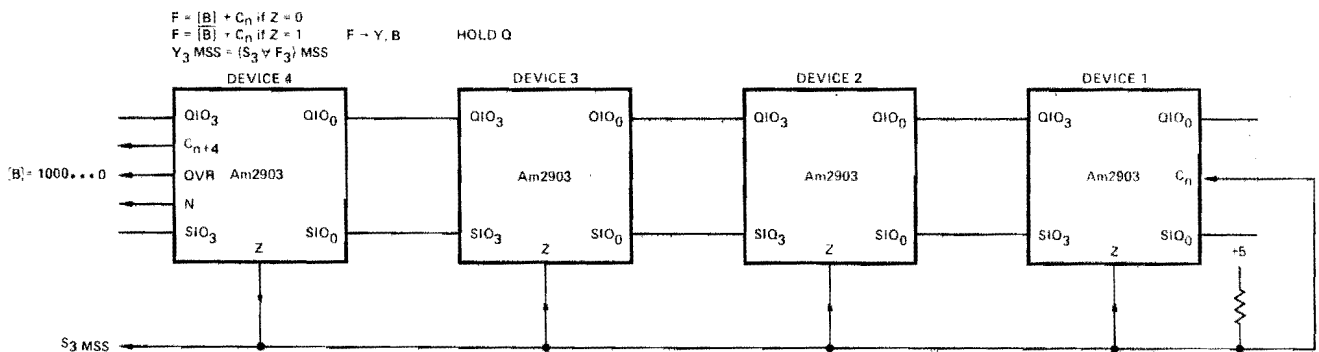


Figure 11. 2's Complement $\leftrightarrow$ Sign/Magnitude.

MPR-045

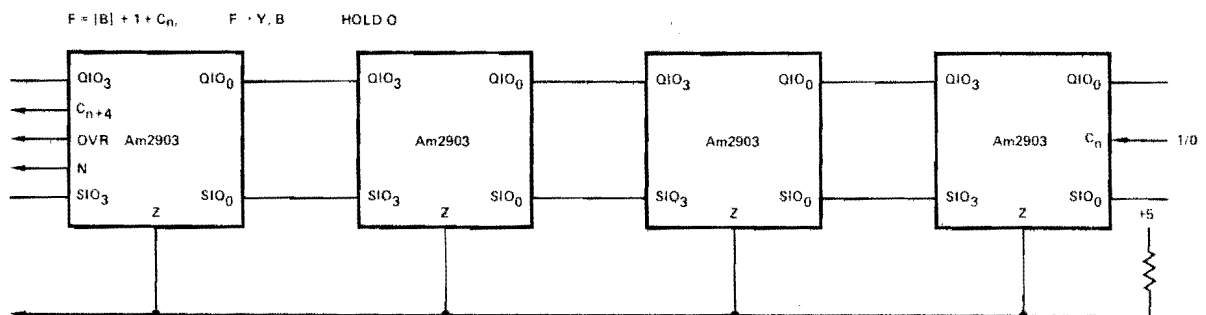
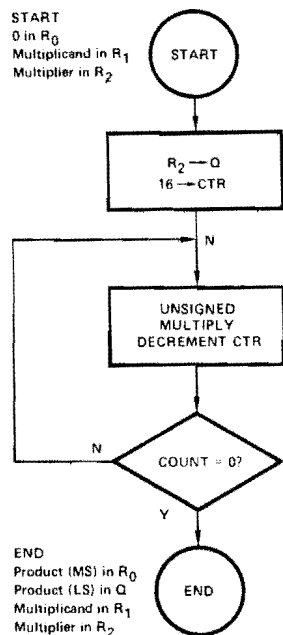


Figure 12. Increment by 2/1.

MPR-046



MPR-047

Figure 13. Unsigned 16 X 16 Multiply Flowchart.

tiplicand (referenced by the A address port) if Z = 1. If Z = 0, the output of the ALU is simply the partial product (referenced by the B address port). Since C_n is held LOW, it is not a factor in the computation. Each positive-going edge of the clock will internally shift the ALU outputs toward the least significant bit and simultaneously store the shifted results in the register selected by the B address port, thus becoming the new partial sum. During the down shifting process, the C_{n+4} generated in device 4 is internally shifted into the Y₃ position of device 4. At this time, one bit of the multiplier will down shift out of the QIO₀ ports of each device into the QIO₃ port of the next less significant slice. The partial product is shifted down between chips in a like manner, between the SIO₀ and SIO₃ ports, with SIO₀ of device 1 being connected to QIO₃ of device 4 for purposes of constructing a 32-bit long register to hold the 32-bit product. At the finish of the 16 x 16 multiply, the most significant 16 bits of the product will be found in the register referenced by the B address lines while the least significant 16 bits are stored in the Q Register. Using a typical Computer Control Unit (CCU), as shown in Figure 16, the unsigned multiply operation requires only two lines of microcode, as shown in Figure 17, and is executed in 17 microcycles.

Two's Complement Multiplication

The algorithm for two's complement multiplication is illustrated by Figure 14. The initial conditions for two's complement multiplication are the same as for the unsigned multiply operation. The Two's Complement Multiply Command is applied for 15 clock cycles in the case of a 16 x 16 multiply. During the down shifting process the term N ∇ OVR generated in device 4 is internally shifted into the Y₃ position of device 4. The data flow shown in Figure 15 is still valid. After 15 cycles, the sign bit of the multiplier is present at the Z output of device 1. At this time, the user must place the Two's Complement Multiply Last cycle command on the instruction lines. On the next positive edge of the clock, the Am2903 will adjust the partial product, if the sign of the multiplier is negative, by subtracting out the two's complement representation of the multiplicand. If the sign bit is positive, the partial product is not adjusted. At this point, two's complement multiplication is completed. Using a typical CCU, as shown in Figure 16, the two's complement multiply operation requires only three lines of microcode, as shown in Figure 19, and is executed in 17 microcycles.

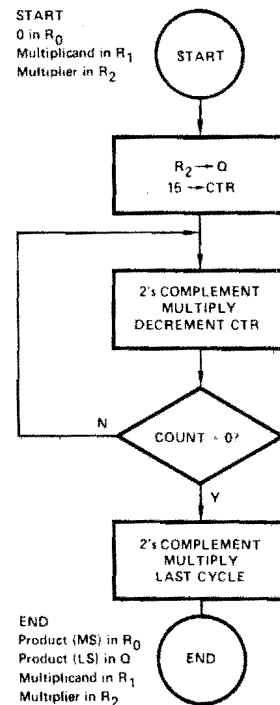


Figure 14. 2's Complement 16 X 16 Multiply.

MPR-048

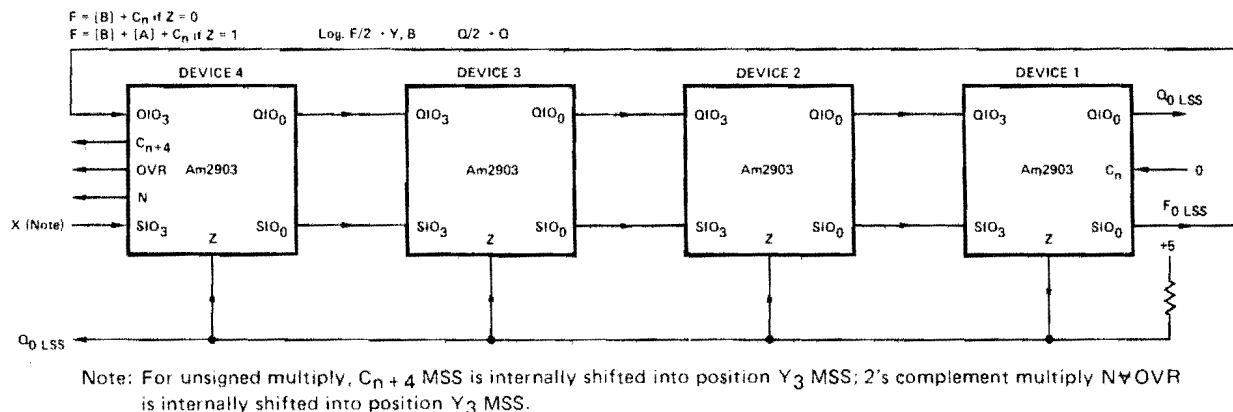


Figure 15. Multiply.

MPR-049

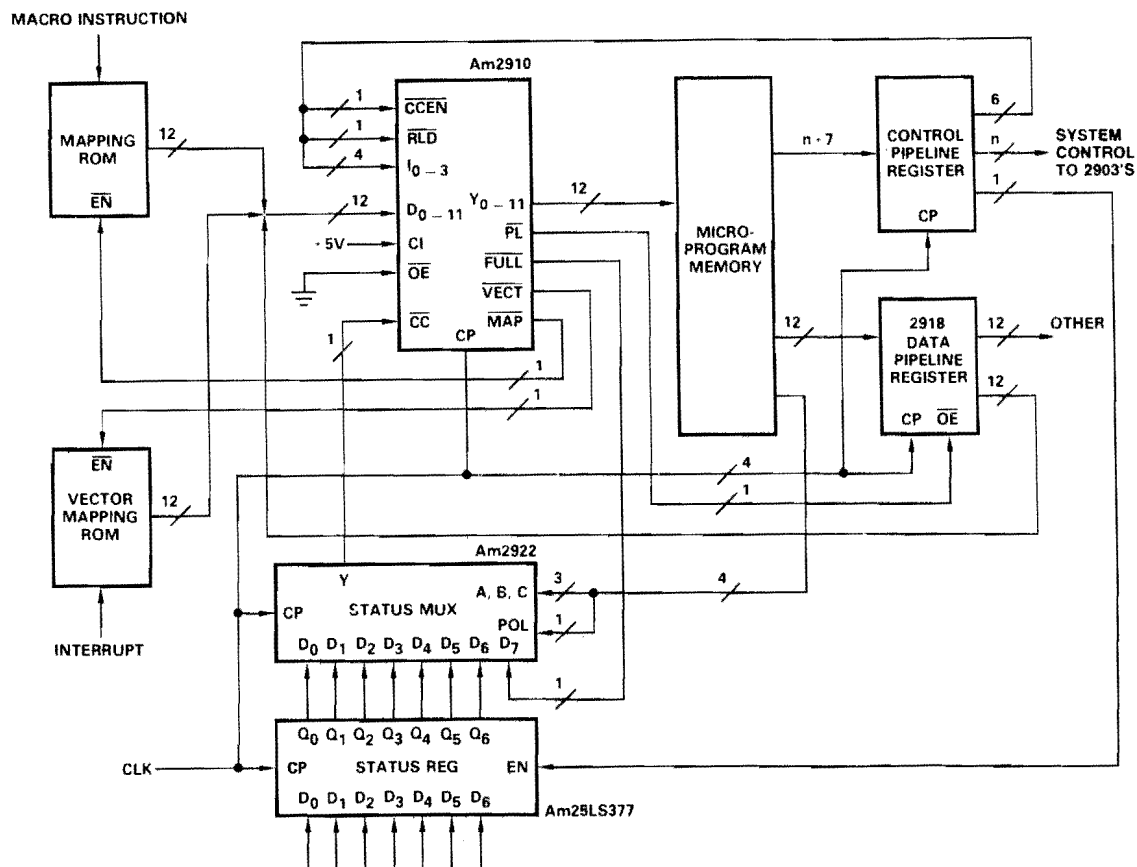
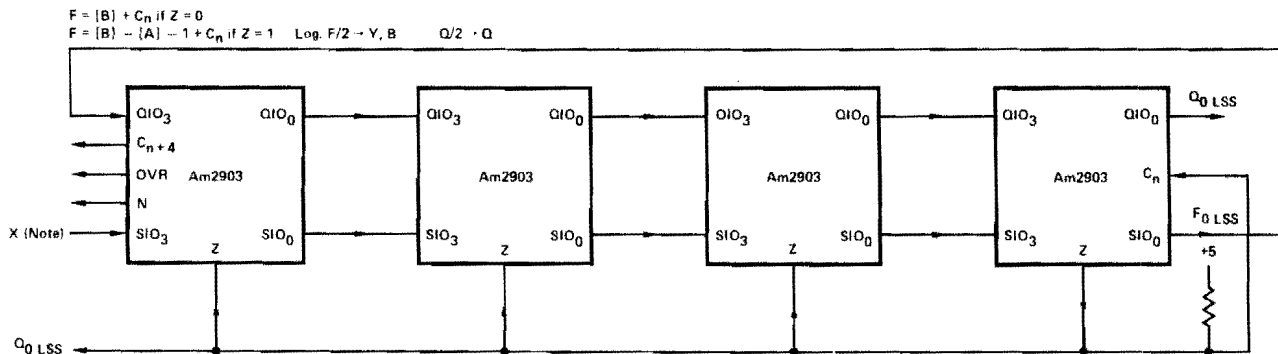


Figure 16. Typical Computer Control Unit (CCU).

MPR-050

Micro Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	I_4-I_1	I_8-I_5	$\overline{OEB}$	$\overline{OEY}$	A_3-A_0	B_3-B_0	C_n	Comment
n	LDCT	00F ₁₆	X	6	6	X	X	R ₂	X	0	Load Counter & R ₂ → Q
n+1	RPCT	n+1	0	0	0	0	0	R ₁	R ₀	0	Unsigned Multiply

Figure 17. Micro Code for Unsigned 16 X 16 Multiply.



Note: N & OVR is internally shifted into position Y₃ MSS.

Figure 18. 2's Complement Multiply, Last Cycle.

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Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	$I_4 - I_1$	$I_8 - I_5$	OEB	OEY	$A_3 - A_0$	$B_3 - B_0$	C_n	Comment
n	LDCT	00E ₁₆	X	6	6	X	X	R ₂	X	0	Load Counter & R ₂ → Q
n+1	RPCT	n+1	0	0	2	0	0	R ₁	R ₀	0	2's Complement Multiply
n+2	X	X	0	0	6	0	0	R ₁	R ₀	Z	2's Complement Multiply (Last Cycle)

Figure 19. Microcode for 2's Complement 16 x 16 Multiply.

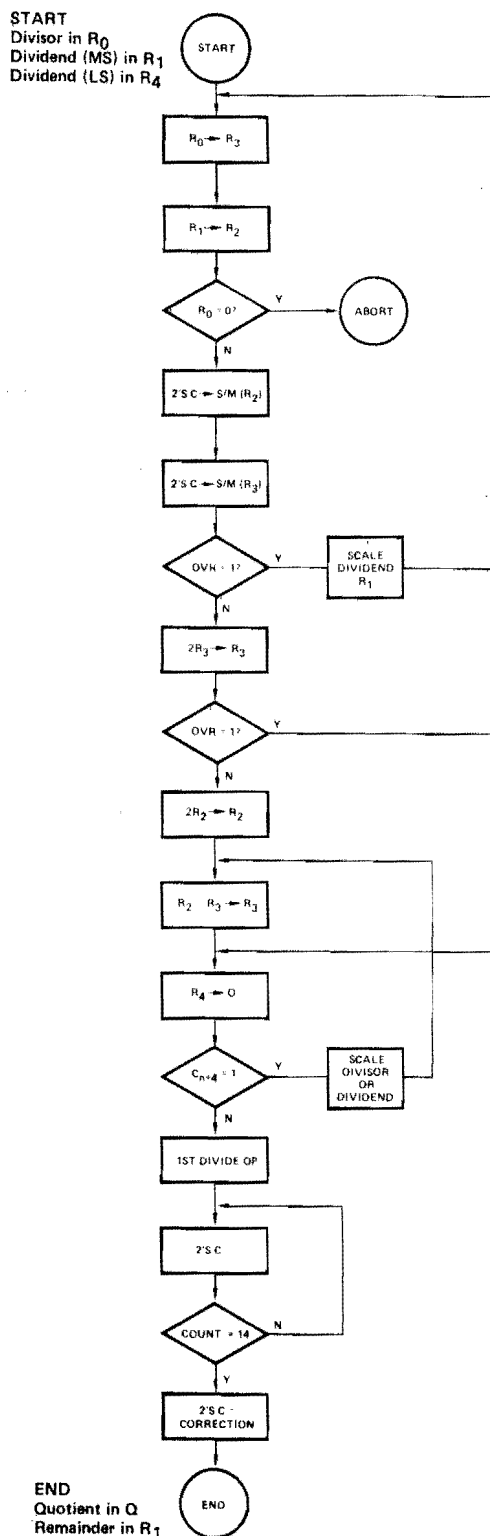


Figure 20. Division Flow Chart – Double Precision Divide.

TWO'S COMPLEMENT DIVISION

The division process is accomplished using a four quadrant non-restoring algorithm which yields an algebraically correct answer such that the divisor times the quotient plus the remainder equals the dividend. The algorithm works for both single precision and multi-precision divide operations. The only condition that needs to be met is that the absolute magnitude of the divisor be greater than the absolute magnitude of the dividend. For multi-precision divide operations the least significant bit of the dividend is truncated. This is necessary if the answer is to be algebraically correct. Bias correction is automatically provided by forcing the least significant bit of the quotient to a one, yet an algebraically correct answer is still maintained. Once the algorithm is completed, the answer may be modified to meet the user's format requirements, such as rounding off or converting the remainder so that its sign is the same as the dividend. These format modifications are accomplished using the standard Am2903 instructions.

The true value of the remainder is equal to the value stored in the working register times 2^{n-1} when n is the number of quotient digits.

The following paragraphs describe a double precision divide operation. The double precision flow chart is based upon the use of the architecture detailed in Figure 16.

Referring to the flow chart outlined in Figure 20, we begin the algorithm with the assumption that the divisor is contained in R₀, while the most significant and least significant halves of the dividend reside in R₁ and R₄ respectively. The first step is to duplicate the divisor by copying the contents of R₀ into R₃. Next the most significant half of the dividend is copied by transferring the contents of R₁ into R₂ while simultaneously checking to ascertain if the divisor (R₀) is zero. If the divisor is zero then division is aborted. If the divisor is not zero, the copy of the most significant half of the dividend in R₂ is converted from its two's complement to its sign magnitude representation. The divisor in R₃ is converted in like manner in the next step, while testing to see if the results of the dividend conversion yielded an indication on the overflow pin of the Am2903. If the output of the overflow pin is a 'one' then the dividend is -2^n and hence is the largest possible number, meaning that it cannot be less than the divisor. What must be done in this case is to scale the dividend by down shifting the upper and lower halves stored in R₁ and R₄ respectively. After scaling, the routine requires that the algorithm be reinitiated at the beginning.

Conversely, if the output of the overflow pin is not a one, the sign magnitude representation of the divisor (R₃) is shifted up in the Am2903, removing the sign while at the same time testing the results of two's complement to sign magnitude conversion of the divisor in the Am2910. If the results of the test indicate that the divisor is -2^n i.e., overflow equals one, then the lower half of the dividend is placed in the Q register

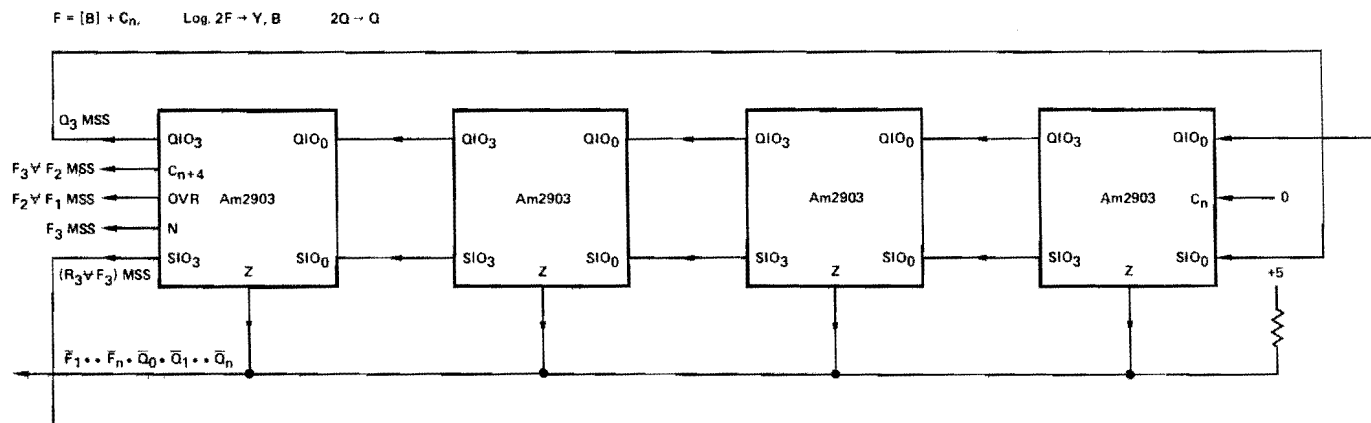


Figure 21. Double Length Normalize/First Divide Operation.

MPR-053

$F = [B] + [A] + C_n \text{ if } Z = 0$
 $F = [B] - [A] - 1 + C_n \text{ if } Z = 1$ $\text{Log. } 2F \rightarrow Y, B$ $2Q \rightarrow Q$

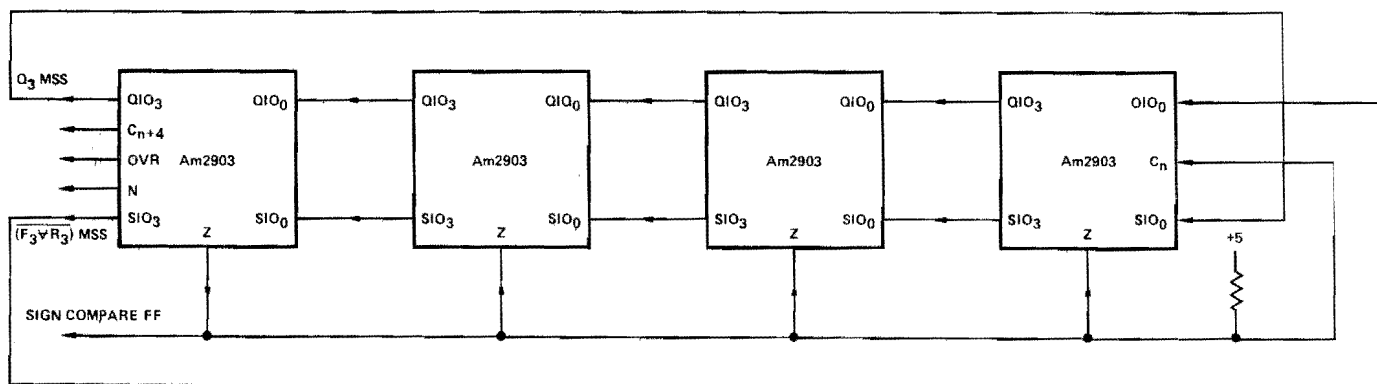


Figure 22. 2's Complement Divide.

MPR-054

$F = [B] + [A] + C_n \text{ if } Z = 0$
 $F = [B] - [A] - 1 + C_n \text{ if } Z = 1$ $F \rightarrow Y, B$ $2Q \rightarrow Q$

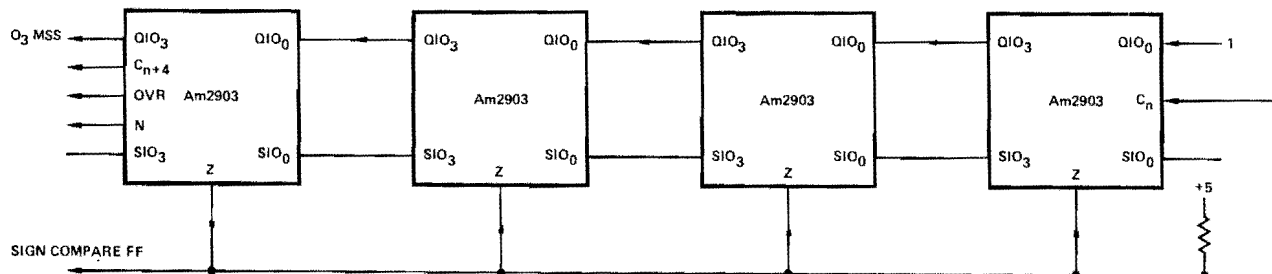


Figure 23. 2's Complement Divide Correction.

MPR-055

and division may proceed. This is possible because the divisor is now guaranteed to be greater than the dividend. If overflow is not a one then we must proceed by shifting out the sign of the sign magnitude representation of the dividend stored in R_2 . At this point we are able to check if the divisor is greater than the dividend by subtracting the absolute value of the divisor (R_3) from the absolute value of the upper half of the dividend (R_2) and storing the results in R_3 . Next, the least

significant half of the dividend is transferred from R_4 to the Q register while simultaneously testing the carry from the result of the divisor/dividend subtraction. If the carry (C_{n+4}) is one, indicating the divisor is not greater than the dividend then a scaling operation must occur. This involves either shifting up the divisor or shifting down the dividend. If the carry is not one then the divisor is greater than the dividend and division may now begin.

Micro Memory Address	Am2910 Inst.	Data Pipeline Reg.	Am2903							Am2922		Comment
			I ₀	I ₄ -I ₁	I ₈ -I ₅	EA	A ₃ -A ₀	B ₃ -B ₀	C _n	SEL	POL	
n	CONT	X	0	6	4	0	R ₀	R ₃	0	X	X	0 R ₀ → R ₃
n+1	CJP	Abort	0	6	4	0	R ₁	R ₂	0	Z	1	X R ₁ → R ₂ , if R ₀ = 0 Abort
n+2	CONT	X	0	0	5	X	X	R ₂	0	X	X	0 2's C to S/M (R ₂)
n+3	CJP	Scale Dividend	0	0	5	X	X	R ₃	0	OVR	1	0 2's C to S/M (R ₃), if OVR ≥ 1, scale
n+4	CJP	n+7	0	4	9	X	X	R ₂	0	OVR	1	X Shift out sign of divisor
n+5	CONT	X	0	4	9	X	X	R ₃	0	X	X	X Shift out sign of divisor
n+6	CONT	X	0	2	F	0	R ₂	R ₃	1	X	X	0 Dividend - Divisor → R ₃
n+7	CJP	Scale Dividend or Divisor	0	6	6	0	R ₄	X	0	C _{n+4}	0	X R ₄ → Q, if Carry = 1, scale
n+8	PUSH	00D ₁₆	0	0	A	0	R ₀	R ₁	0	0	1	X Loop set up & First Divide Operation
n+9	RFCT	X	0	0	C	0	R ₀	R ₁	Z	X	X	X Test Loop Count & 2's C Divide
n+A	CONT	X	0	0	E	0	R ₀	R ₁	Z	X	X	X 2's C Divide Correction

Figure 24. Microcode for Double Precision Divide.

The first divide operation is used to ascertain the sign bit of the quotient. The two's complement divide instruction is then executed repetitively, fourteen times in the case of a sixteen bit divisor and a thirty-two bit dividend. The final step is the two's complement correction command which adjusts the quotient by allowing the least significant bit of the quotient to be set to one. At the end of the division algorithm the sixteen bit quotient is found in the Q register while the remainder now replaces the most significant half of the dividend in R₁. It should be noted that the remainder must be shifted down fifteen places to represent its true value. The interconnections for these instructions are shown in Figures 21, 22, 23. Using a typical CCU as shown in Figure 16, the double precision divide operation requires only eleven lines of microcode, as shown in Figure 24.

For those applications that require truncation instead of bias correction, the same algorithm as above should be implemented except one additional Two's Complement Divide instruction should be used in lieu of the Two's Complement Divide Correction and Remainder instruction. However, this technique results in an invalid remainder.

It is possible to do multiple-precision divide operations beyond the double precision divide shown above. For example, to do a triple precision divide for a 16-bit CPU, the upper two thirds of the dividend are stored in R₁ and Q as in the case for double precision divide. The lower third of the dividend is stored in a scratch register, R₅. After checking that the magnitude of the divisor is greater than the magnitude of the dividend, using the same tests as defined in Figure 20, the procedure is as follows:

1. Execute a Double Length Normalize/First Divide Operation instruction.
2. Execute the Two's Complement Divide instruction fifteen times.
3. Transfer the contents of Q, the most significant half of the quotient, to R₂.
4. Transfer R₅ to Q.
5. Execute the Two's Complement Divide instruction fifteen times.
6. Execute the Two's Complement Divide Correction and Remainder instruction.

The upper half of the quotient is then in R₂, the lower half of the quotient is in Q and the remainder is in R₁. The flow chart for this is shown in Figure 25. This technique can be expanded for any precision which is required.

Byte Swap

The multi-port architecture of the Am2903 allows for easy implementation of high- and low-order byte swapping. Figure 26 outlines a byte swap implementation utilizing two data ports. Initially, the lower order 8-bit byte is stored in devices 1 and 2, while the high-order byte is in devices 3 and 4. When the user wishes to exchange the two bytes, the register location of the desired word is placed on the B address port. When the byte swap line is brought LOW, the bytes to be swapped will be flowing from the DB ports of the Am2903 through the Am25LS240/244 Three-state Buffers. The outputs of the

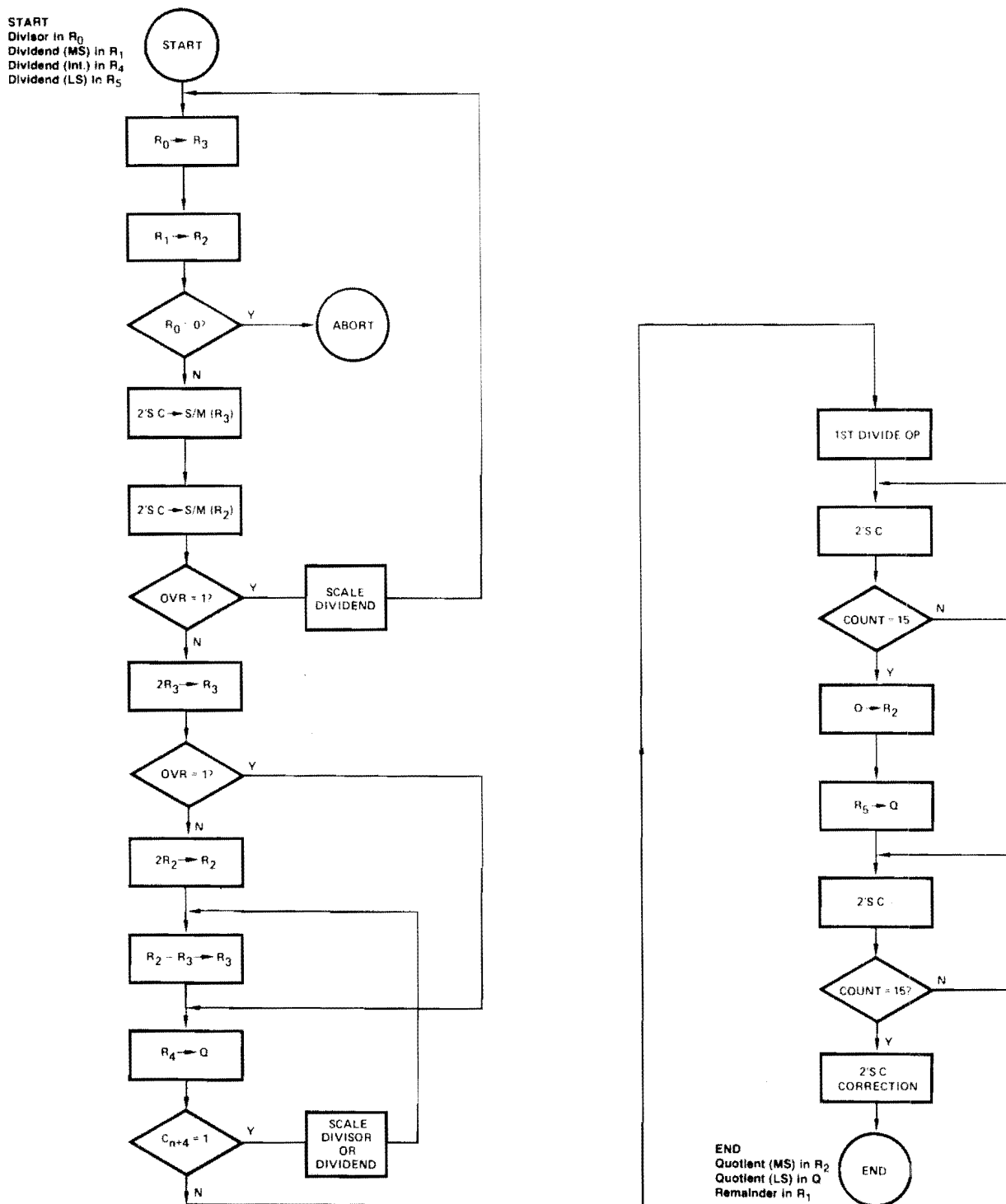


Figure 25. Division Flow Chart - Triple Precision Divide.

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three-state buffers are permuted such that the byte swap is achieved. The resultant permuted data is presented to the DA ports of the Am2903 where it is re-loaded into the memories of the Am2903 on the next positive edge of CP using the source and function commands of $F = \bar{A}$ plus C_n ($C_n = 0$) for the Am25LS240 or $F = A$ plus C_n ($C_n = 0$) for the Am25LS244 and the destination command $F \rightarrow Y, B$.

A higher speed technique for achieving the byte swap operation is illustrated in Figure 27. Instead of inputting the permuted data via the DA ports, the permuted data is inputted via the Y input/output ports with $\overline{OE}_Y$ held HIGH. This technique bypasses the ALU, thus allowing faster operation. The Am2903 destination command $F \rightarrow Y, B$ should be used.

Memory Expansion

The Am2903 allows for a theoretically infinite memory expansion. Figure 28 pictures a 4-bit slice of a system which has 48 words of RAM and 16 words of ROM. RAM storage is provided by the Am2903 and the Am29705's. The Am29705 RAM is functionally identical to the Am2903 RAM. The Am29751A is used to store constants and masks and is addressable from address port A only. The system is organized around five data buses. Inter-bus communication may be done through the Am29705's or the

Am2903. The memory addressing scheme specifies the data source for the R input of the ALU emanating from the register locations specified by address field A. A_0-3 addresses 16 memory locations in each chip while address bits A_4-6 are decoded and used for the output enable for the desired chip. The B address field is used to select the S input of the ALU and the C field is used to specify the register location where the result of the ALU operation is to be stored.

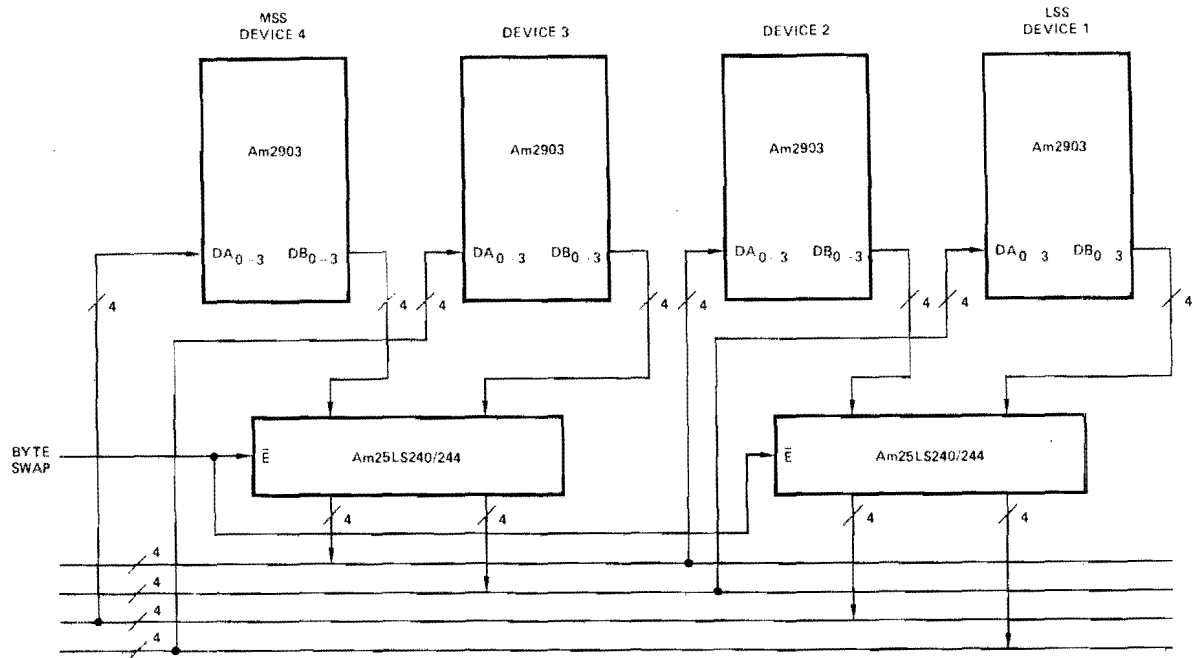


Figure 26. Byte Swap.

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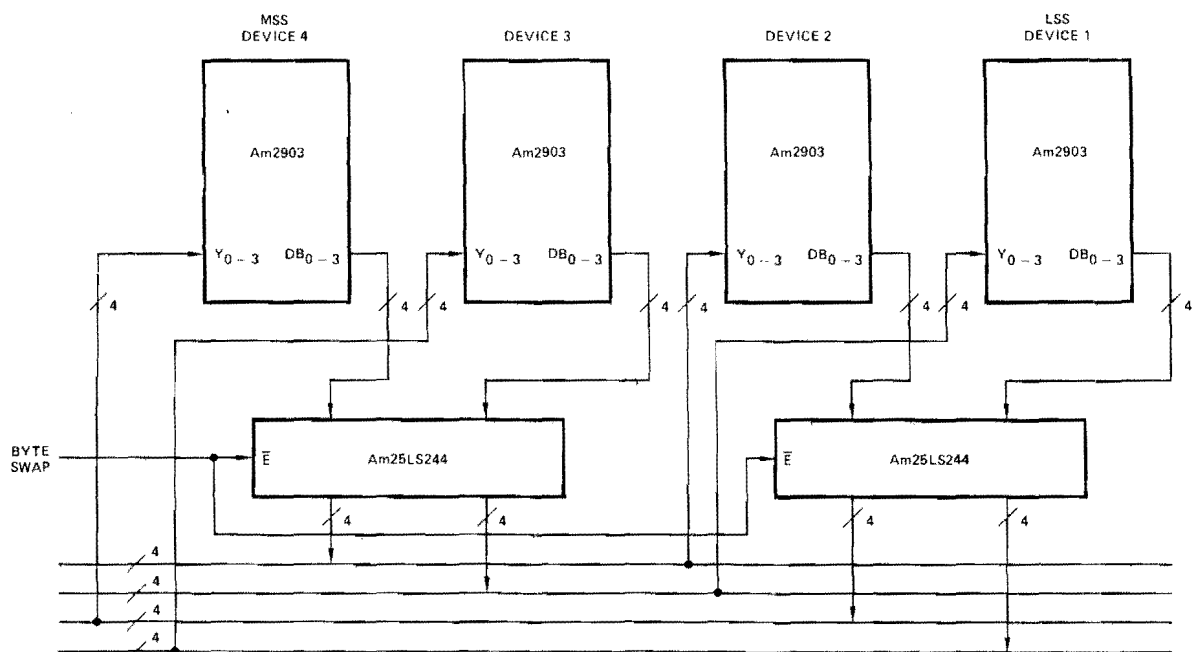


Figure 27. High Speed Byte Swap.

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latched and the destination address is now selected for use by the RAM address lines. When the destination address stabilizes on the address lines, the $\overline{\text{IEN}}$ pin is brought LOW. The $\overline{\text{WRITE}}$ output of the Am2903 will now go LOW, enabling the decoder sourced by address bits C_4 and C_5 . The selected decoder line will go LOW, allowing the desired memory location to be written into. To switch between two- and three-address architecture, the user simply makes the source and destination addresses the same; i.e., $B_{0-3} = C_{0-3}$. For two-address architecture, the MUX is removed from the circuit and $B_{4-5} = C_{4-5}$.

